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SAMSUNG DISPLAY

Confidential

Date : 19th.July.2013

# Specification for Approval

**Product Name : 4.65" HD AMOLED For GIONEE**

**Model Name : AMS465GS53**

**Description : 4.65" HD (720*1280) 16M Color**

| Proposed by | | | Customer's Approval |
|---|---|---|---|
| Designed | Checked | Approved | |
| SW CHEGAL | JS LEE | MH LEE | |

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제갈승원/12408853/제품개발2그룹(OLED)/119310365/20130720081253

395061374275368

# Revision History

| Date | Rev. No. | Contents | Remark |
|---|---|---|---|
| May.27.'13 | Draft 0.0 | -.Initial issue | |
| June.20.'13 | V0.1 | .Add the WAD value.<br>(White Angular Distortion)<br>.Change Contrast condition.<br>: 270nit → 300nit<br>.Change the γ value<br>.Change the TSP Parts list<br>: FPCB, IC Part . | Page 9<br>Page 10<br>Page 19<br>Page 62 |
| July.01 '13 | V0.2 | -.Change the Window inspect condition<br>: 90°(Z) ± 5° → 90°(Z) ± 30° | Page 44 |
| July.19 '13 | V0.3 | .Change the Align tolerance of the FPCA.<br>: 0.35 → 0.5 | Page 56 |

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# 1. Scope

This Specification defines general provisions as well as inspection standards for AMOLED module supplied by SAMSUNG Display Co., LTD.,
If the event of unforeseen problems or unspecified items occurs, we naturally shall negotiate and agree to solution with customer.

# 2. Warranty

Basically, warranty term is 12 months of reliability characteristics of quality level after the outgoing date in SAMSUNG Display Co., LTD., and SAMSUNG Display Co., LTD., could compensate for defectives which happens within warranty term under condition that the products should be stored or be used as specified under normal condition within the contents of specification.
Otherwise, it is impossible to compensate for defectives when they happens by customer's mistake such as careless handing or circuit change, etc.
And after 12 months of warranty term, all replacements for defectives will be charged.

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## 3. Features

1) Display Color : 16M Color
2) Display Format : 4.65" HD720 : 720x1280
3) Interface : DSI 4-lane
4) Driver IC : S6E8AA0-A01 ( SEC )
5) Touch IC : MMS144 ( Melfas )
6) Polarizer : Hard Coating Polarizer

## 4. Mechanical Specification

| Item | Specifications | Unit |
|---|---|---|
| Dimensional outline | 66.36(W) x 131.8(H) x 2.126(T) | mm |
| Glass outline | 62.36(W) x 111.32(H) x 0.8(T) | mm |
| Number of dots | 720(W) x RG(BG) x 1280(H) | Dots |
| Active area | 57.96(W) X 103.04(H) | mm |
| Diagonal Inch | 4.65 | inch |
| Pixel pitch | 161(W) X 161(H) | um |
| Glass Thickness | 0.3 (LTPS)<br>0.5 (Encap) | mm |

## 5. Maximum Rating

| Item | | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage (Display) | Logic | VCI | -0.3 | 5.0 | V | (1),(2) |
| | | VDD3 | -0.3 | 5.0 | V | (1),(2) |
| | Power | VBAT | -0.3 | 6.0 | V | (3) |
| | | ELVDD | -0.3 | 6.0 | V | (1),(2),(3) |
| | | ELVSS | -10 | AGND+0.3 | V | (1),(2),(3) |
| Supply voltage (TSP) | Logic | TSP_VDD | -0.3 | 3.6 | V | (1),(2) |
| | Power | TSP_AVDD | -0.3 | 3.6 | V | (1),(2) |
| Input voltage | | VI | -0.3 | VDD3+0.5 | V | (2) |
| Operating temperature | | Top | -20 | 60 | ℃ | - |
| Storage temperature | | Tstg | -30 | 70 | ℃ | - |
| Humidity | | Hstg | 10 | 90 | %RH | |

Note 1) Supply voltage should satisfy the below condition of
VCI, VDD3, TSP_AVDD and TSP_VDD > VSS (GND).
Note 2) If the supplied voltage exceeds the maximum limitation, LSI can be damaged permanently.
Therefore, while operating, it is recommend to use LSI within the maximum electrical limitation.
If not, LSI can cause decreased reliability or operational problems.
Note 3) VBAT is input supply to DCDC IC which is mounted on SET board.
And ELVDD and ELVSS, which are supply voltage for display, are output power from DCDC IC.

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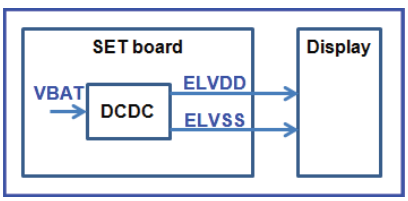
# 6. Electrical Characteristics

-. Test Conditions: VDD3=2.2V VCI=3.1V, VSS=0V, VBAT=3.8V
Temp=25℃ unless otherwise specified.

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Supply voltage (Display) | Logic Voltage | VDD3 | - | 2.1 | 2.2 | 3.3 | V | 3) |
| | Analog Voltage | VCI | - | 3.0 | 3.1 | 3.6 | | |
| | Battery Supply Voltage | VBAT | - | 3.42 | 3.8 | 4.18 | | 1) |
| Supply voltage (TSP) | Analog Voltage | TSP_AVDD | - | 3.2 | 3.3 | 3.4 | V | |
| Logic Input Voltage (Display) | "H" level | VIH | - | 0.7*VDD3 | - | VDD3 | V | |
| | "L" level | VIL | - | 0.0 | - | 0.3*VDD3 | | |
| Logic Output Voltage (Display) | "H" level | VOH | IOH = -0.1mA IOL = 0.1mA | 0.8*VDD3 | - | VDD3 | V | |
| | "L" level | VOL | | 0.0 | - | 0.2*VDD3 | | |
| Logic Input Voltage (TSP) | "H" level | VIH | - | 0.7*TSP_VDD | - | TSP_VDD +0.5 | V | |
| | "L" level | VIL | - | -0.5 | - | 0.3*TSP_VDD | | |
| Logic Output Voltage (TSP) | "H" level | VOH | IOH = -0.1mA IOL = 0.1mA | 0.8*TSP_VDD | - | TSP_VDD | V | |
| | "L" level | VOL | | 0.0 | - | 0.2*TSP_VDD | | |
| Logic Current | "H" level | IIH | VI=VDD3, TSP_VDD or VSS | | - | 10.0 | uA | |
| | "L" level | IIL | | -10.0 | - | | uA | |
| Current Consumption | Sleep out mode Display mode | ICI | Frame frequency 60Hz, white pattern | - | 30 | 60 | mA | |
| | | IVDD3 | | - | 40 | 80 | mA | |
| | | IBAT | | - | 410 | 540 | | 1),2) |
| | Sleep in mode | ICI | sleep mode, EL_ON="0" | - | - | 60 | uA | |
| | | IVDD3 | | | - | 100 | uA | |
| | | IBAT | | - | - | 100 | uA | 1),2) |
| Frame Frequency | | $f_{FRM}$ | - | - | 60 | - | Hz | |

Note 1) VBAT is input supply to DCDC IC mounted on SET board.
Note 2) IBAT is measured at DCDC input (VBAT) on test JIG
Current can vary according to DC DC efficiency and circuit layout
Note 3) RESET level should be the same as VDD3

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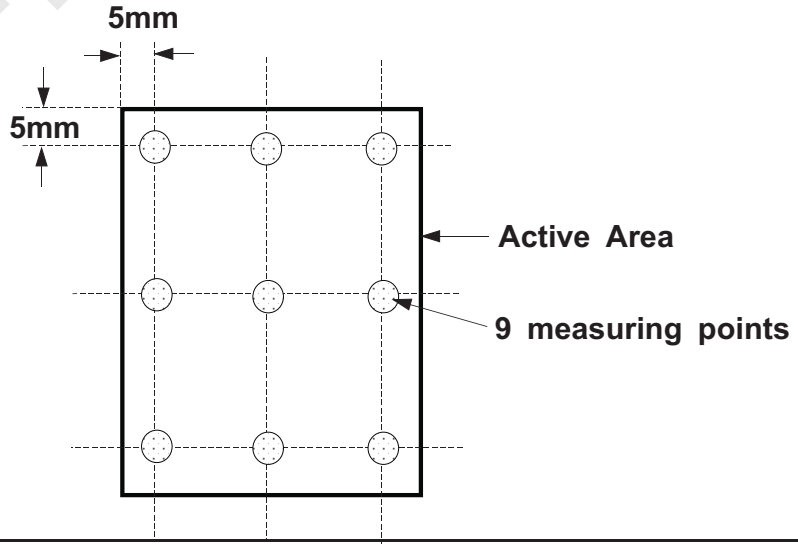
## 7. Electro-optical characteristics

| Item | | Symbol | Temp | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| Brightness | | | 25℃ | Normal (White Mode) | 240 | 300 | 360 | cd/m$^2$ | Center brightness |
| Uniformity | | | 25℃ | Normal (White Mode) | 75 | - | - | % | (1) |
| Contrast ratio | | K | 25℃ | Φ=0°,θ=0° | 3,400 | - | - | - | (1),(2) |
| Color of CIE coordinate | White | x | 25℃ | Φ=0° θ=0° | 0.283 | 0.313 | 0.343 | - | (1),(2),(3) |
| | | y | | | 0.299 | 0.329 | 0.359 | - | |
| | Red | x | | | 0.640 | 0.670 | 0.700 | - | |
| | | y | | | 0.299 | 0.329 | 0.359 | - | |
| | Green | x | | | 0.170 | 0.220 | 0.270 | - | |
| | | y | | | 0.676 | 0.726 | 0.776 | - | |
| | Blue | x | | | 0.103 | 0.143 | 0.183 | - | |
| | | y | | | 0.015 | 0.055 | 0.095 | - | |
| Color Gamut | | | 25℃ | vs. NTSC | 85 | (100) | - | % | |
| Viewing angle | | | 25℃ | Up/Down/Right/Left CR ratio ≥10 | 80 | - | - | ° | |
| Cross Talk | | | 25℃ | window: 4% white/black background: gray117 | - | - | 3 | % | (4) |
| Gamma | | | 25℃ | Log(Lv-Lb)=Ylog(V)+log(a) V(Gray)= 48,72,104,132, 164,192,224,252,255 Lum(gray255)=300nit | 1.9 | 2.2 | 2.5 | - | |
| WAD (White Angular Distortion) | | Δx | 25℃ | Φ=30° | -0.04 | - | 0.04 | - | (5) |
| | | Δy | | | -0.04 | - | 0.04 | - | |

Above optical characteristics are guaranteed only for 300nit(brightness).

Note 1) Uniformity Measuring Point

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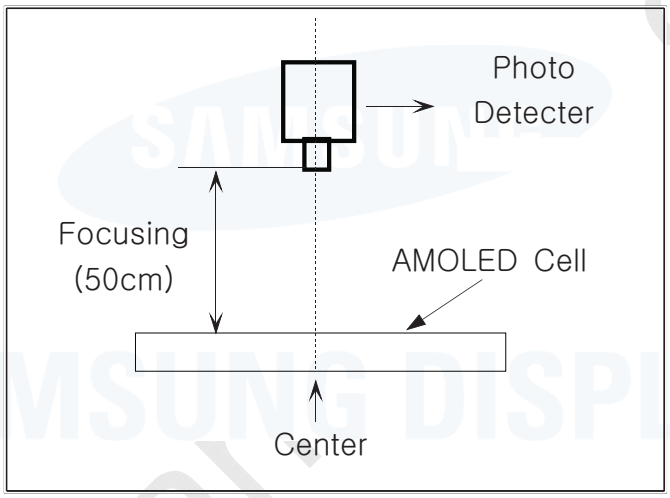
**Uniformity = Lmin / Lmax * 100 [%]**

Note 2) Definition of contrast ratio (K)

$$\text{Contrast Ratio(K)} = \frac{\text{Brightness of selected dot (White patterned area) at 300cd/m}^2}{\text{Brightness of non-selected dot (Black patterned area) at 300cd/m}^2}$$

Note 3) Optical measuring system
temperature regulated chamber




Note 4) Cross Talk
a. measure luminance at the position, $P_0$.
b. calculate cross talk as below equation.

$$L_{W\ OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

$$L_{B\ OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$crosstlak = \frac{\left| L_{Wi\ ON} - L_{W\ OFF} \right|}{L_{W\ OFF}} \times 100\% \quad \text{(i = 5 to 8 )}$$

$$crosstlak = \frac{\left| L_{Bi\ ON} - L_{B\ OFF} \right|}{L_{B\ OFF}} \times 100\% \quad \text{(i = 5 to 8 )}$$

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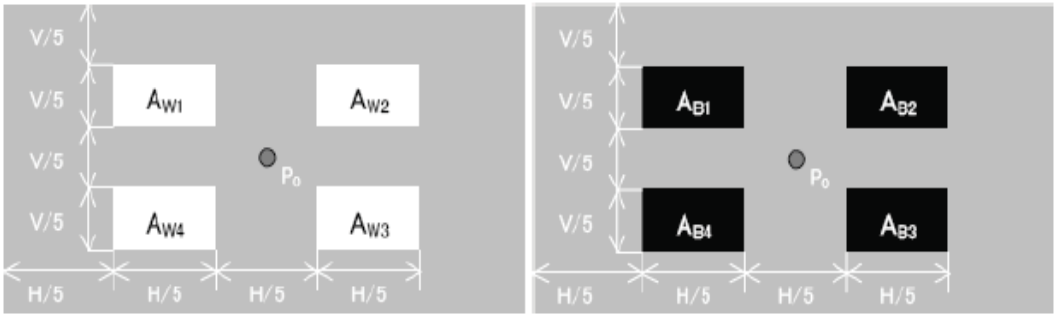
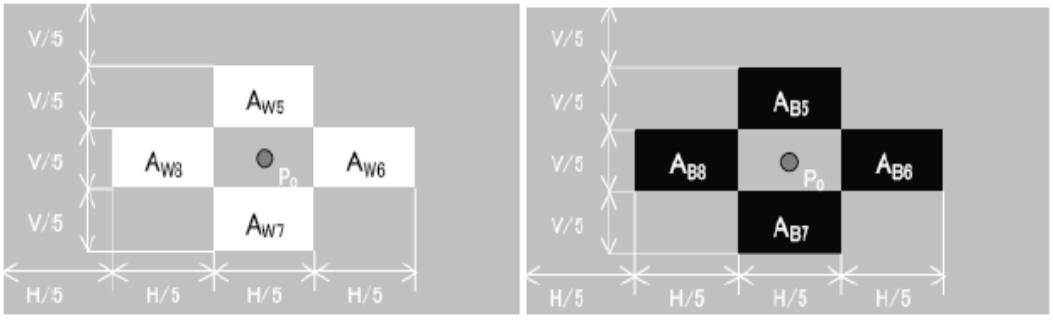
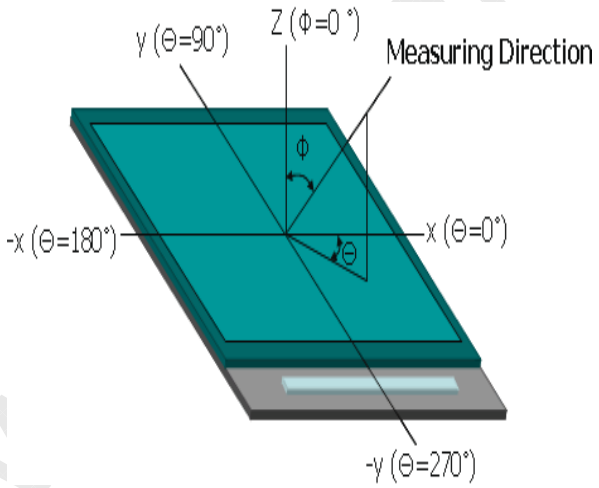



(a) $L_{W\ OFF}$, $L_{B\ OFF}$ measuring pattern




(b) $L_{W\ ON}$, $L_{B\ ON}$ measuring pattern

Note 5) Definition of Φ, θ



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# 8. I/O Connection & Block Diagram

## 8-1. I/O Connection

| No. | Name | I/O | Description |
|---|---|---|---|
| 1 | GND | Ground | Ground |
| 2 | GND | Ground | Ground |
| 3 | D3_N | I/O | Fourth differential data input/output pin |
| 4 | RESX | I | Display reset. Active low. |
| 5 | D3_P | I/O | Fourth differential data input/output pin |
| 6 | NC | Not Connected | |
| 7 | GND | Ground | Ground |
| 8 | VDD3 | Power | Power supply for display logic circuit |
| 9 | D0_N | I | First differential data input/output pin |
| 10 | VCI | Power | Power supply for display analog circuit |
| 11 | D0_P | I/O | First differential data input/output pin |
| 12 | TSP_VDD | Power | Power supply for touch analog circuit |
| 13 | GND | Ground | Ground |
| 14 | MTPHV | Power | Power supply for MTP Programming or Erase<br>Open or connected to GND |
| 15 | CLK_N | I | Differential clock input |
| 16 | EL_ON | I | DC-DC Enable |
| 17 | CLK_P | I | Differential clock input |
| 18 | NC | Not Connected | |
| 19 | GND | Ground | Ground |
| 20 | GND | Ground | Ground |
| 21 | D1_N | I/O | Second differential data input/output pin |
| 22 | TSP_SCL | I | Touch I2C clock input p |
| 23 | D1_P | I/O | Second differential data input/output pin |
| 24 | TSP_SDA | I/O | Touch I2C data input/output pin |
| 25 | GND | Ground | Ground |
| 26 | GND | Ground | Ground |
| 27 | D2_N | I/O | Third differential data input/output pin |
| 28 | TSP_INT | O | Touch Interrupt |
| 29 | D2_P | I/O | Third differential data input/output pin |
| 30 | GND | Ground | Ground |
| 31 | GND | Ground | Ground |
| 32 | GND | Ground | Ground |
| 33 | NC | Not Connected | |
| 34 | NC | Not Connected | |
| 35 | ELVDD | Power | Positive power supply for EL |
| 36 | ELVSS | Power | Negative power supply for EL |
| 37 | ELVDD | Power | Positive power supply for EL |
| 38 | ELVSS | Power | Negative power supply for EL |
| 39 | ELVDD | Power | Positive power supply for EL |
| 40 | ELVSS | Power | Negative power supply for EL |

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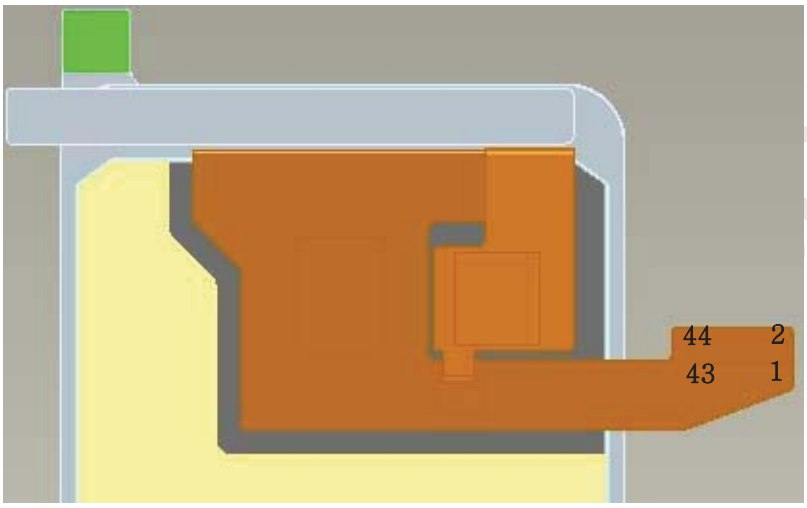
| No. | Name | I/O | Description |
|---|---|---|---|
| 41 | NC | Not Connected | |
| 42 | NC | Not Connected | |
| 43 | GND | Ground | Ground |
| 44 | GND | Ground | Ground |




**Pin layout of B-to-B contact pads**

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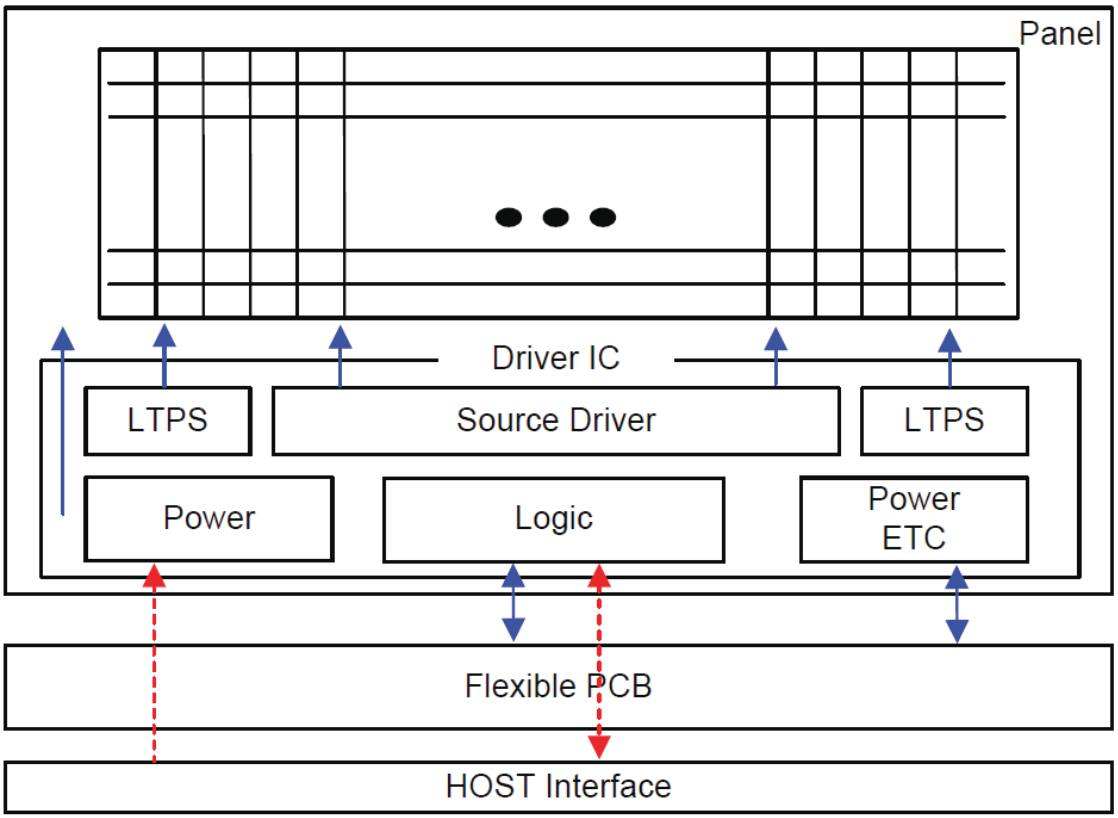
## 8-2. Circuit block diagram (Display)




Level I Interface signals
Level II Interface signals

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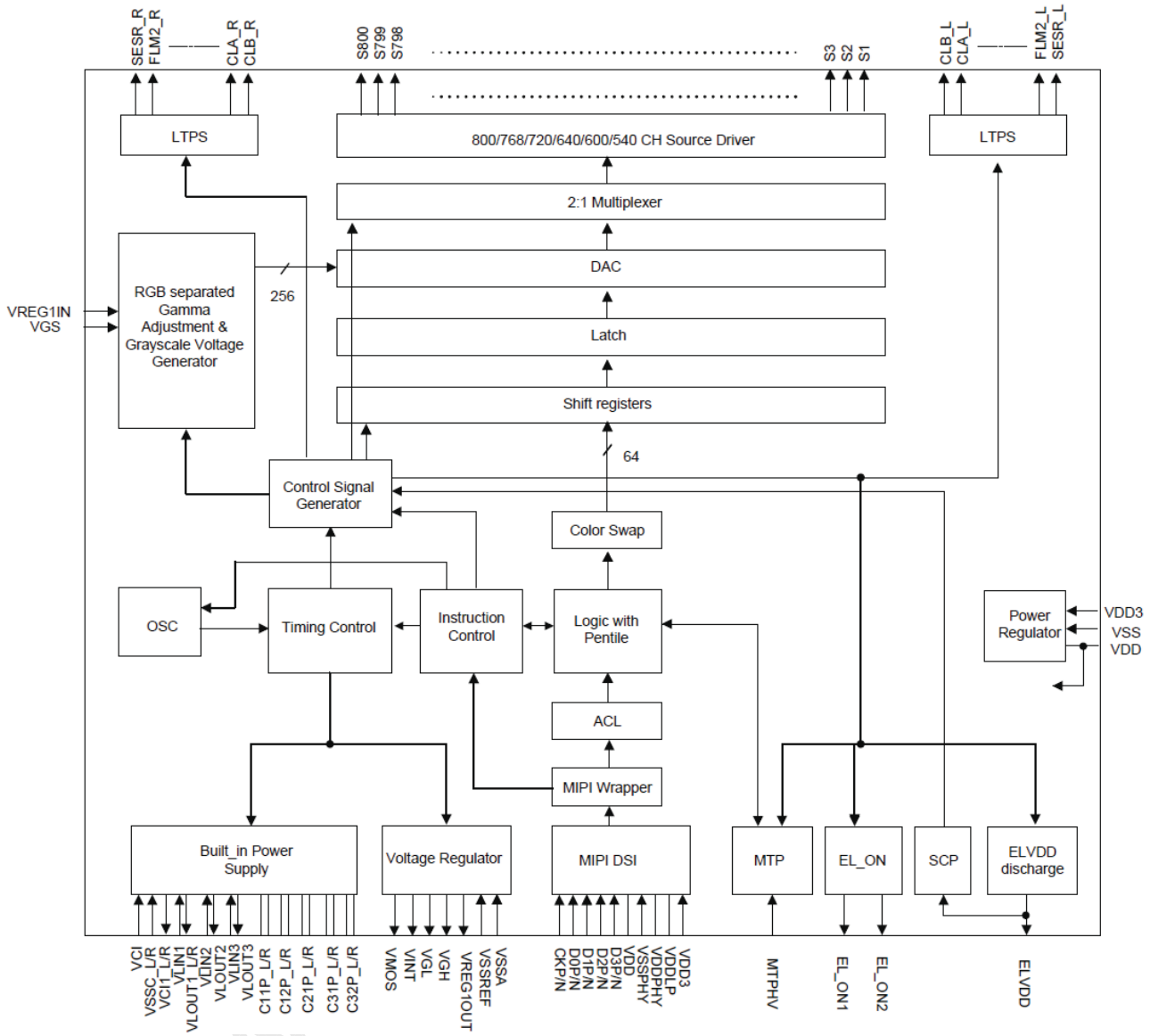
## 8-3. Circuit block diagram (Driver IC for display)

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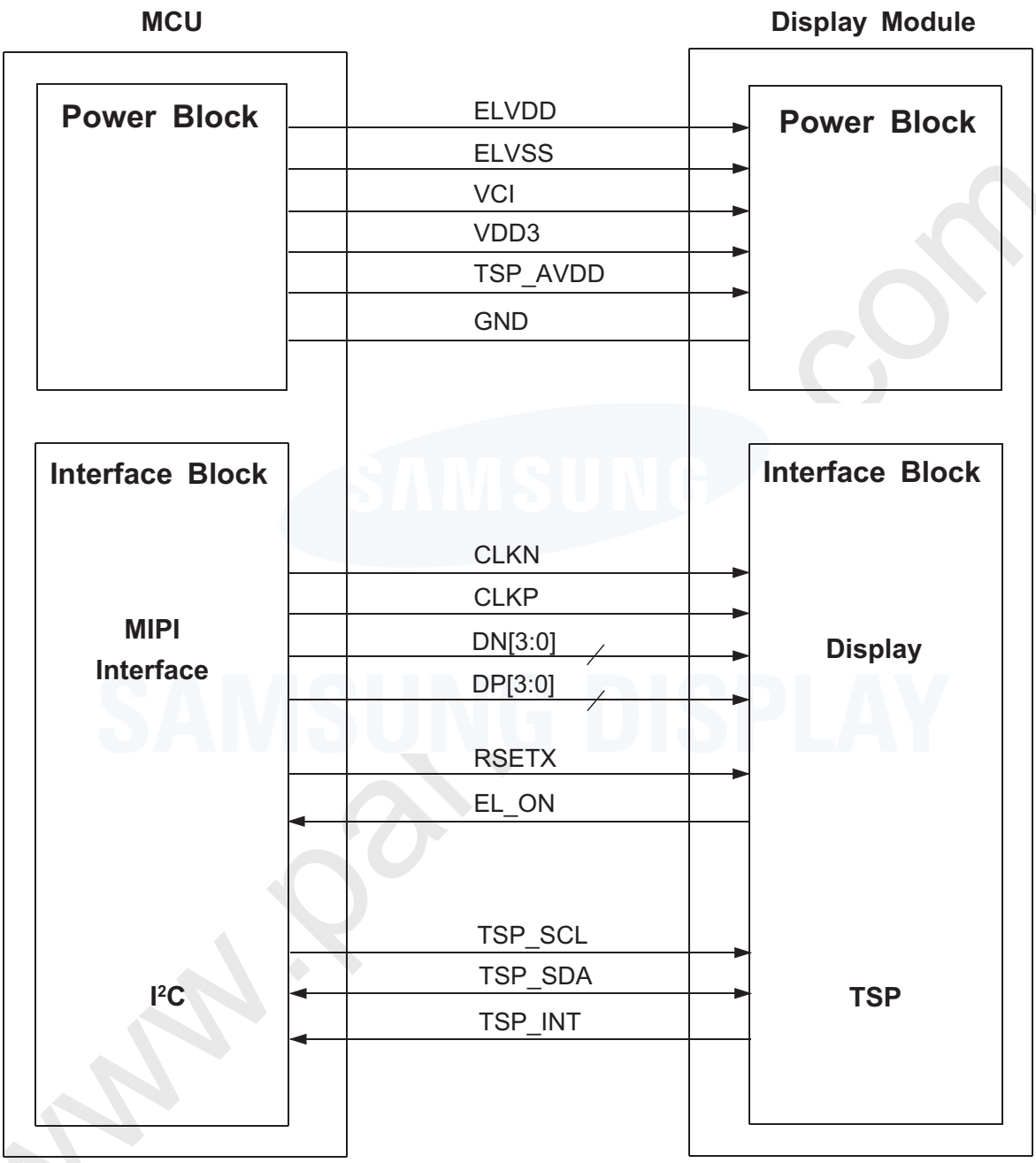
## 8-4. MCU and Display Module Interface Configuration

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# 9. Recommended Operating Sequence

## 9-1. Power ON/OFF sequence

### [ Power On Sequence ]

START

**[ System Power On ]**
turn-On VBAT / VDD3 / VCI

Wait 25ms

**[ H/W RESET Release ]**
System Reset

Wait 5ms

**[1] LEVEL2/MTP key Enable**
(Refer to Next Page in detail)

**MIPI Signal On** (MIPI CLK→HS)

**Sleep out Command** (11h)

Wait 5ms

**ID 1(A2h) / 2(53h) / 3 Read** (D1h)

**[2] Panel Condition Set**
(Refer to Next Page in detail)

**[3] Gamma condition Set**
(Refer to Next Page in detail)

**[4] ETC Condition Set**
(Refer to Next Page in detail)

**[5] ELVSS set**
(Refer to Next Page in detail)

**[6] ACL Control set**
(Refer to Next Page in detail)

Wait 120ms

**Display On Command** (29h)

**Display On State**

### [ Power Off Sequence ]

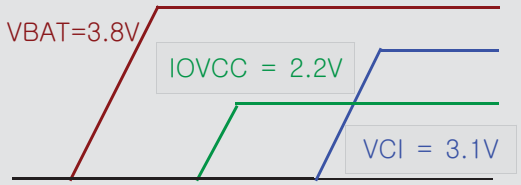
**Display Off Command** (28h)

**Sleep in Command** (10h)

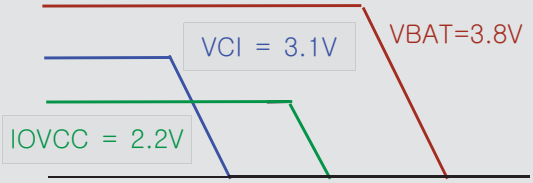
Wait 120ms

**[ System Power Off ]**
turn-OFF VCI / VDD3 /VBAT

**[ System Power On Sequence ]**
VBAT→VDD3→VCI or Simultaneously




**[ System Power OFF Sequence ]**
VCI→VDD3→VBAT or Simultaneously

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## [1] LEVEL2 Command Set

| Command | Parameter | | Description |
|---|---|---|---|
| F0h | 1st | 5Ah | LEVEL2 Command Enable |
| | 2nd | 5Ah | |
| F1h | 1st | 5Ah | MTP Key Enable |
| | 2nd | 5Ah | |

## [2] Panel Condition Set (HS_Clock 480Mbps)

| Command | Parameter | | Description |
|---|---|---|---|
| F8h (Foward) | 1st | 3Dh | DOTC |
| | 2nd | 35h | FLTE |
| | 3rd | 00h | FLTEH |
| | 4th | 00h | FLTE2 |
| | 5th | 00h | FLTE2_H |
| | 6th | 93h | FLWE |
| | 7th | 00h | FLWE2 |
| | 8th | 3Ch | SCTE |
| | 9th | 7Dh | SCWE |
| | 10th | 08h | INTE |
| | 11th | 27h | INWE |
| | 12th | 7Dh | E_INTE |
| | 13th | 3Fh | E_INWE |
| | 14th | 00h | EMPS |
| | 15th | 00h | E_FLTE |
| | 16th | 00h | E_FLTE_H |
| | 17th | 20h | E_FLWE |
| | 18th | 04h | E_FLWE_H |
| | 19th | 08h | E_SCTE |
| | 20th | 6Eh | E_SCWE |
| | 21st | 00h | A_FLTE |
| | 22nd | 00h | A_FLTE_H |
| | 23rd | 00h | A_FLWE2 |
| | 24th | 02h | A_FLWE_H |
| | 25th | 08h | CLTE |
| | 26th | 08h | SHE |
| | 27th | 23h | CLWEA |
| | 28th | 23h | CLWEB |
| | 29th | C0h | FLM_DC |
| | 30th | C8h | CLK1_DC |
| | 31st | 08h | INT1_DC |
| | 32nd | 48h | BICTL_DC |

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| Command | Parameter | | Description |
|---|---|---|---|
| F8h (Foward) Contonued | 33rd | C1h | CLA_DC |
| | 34th | 00h | SESR_DC |
| | 35th | C1h | ACL_FLM_DC |
| | 36th | FFh | EM_CLK1_DC |
| | 37th | FFh | EM_CLK2_DC |
| | 38th | C8h | EM_INT1_DC |
| F2h | 1st | 80h | Display area |
| | 2nd | 03h | VBP : 3 HSYNC |
| | 3rd | 0Dh | VFP : 13 HSYNC |

## [3] Gamma Condition Set

1) Gamma set ( Typ 300cd )

| Command | Parameter | | Description |
|---|---|---|---|
| FAh | 1st | 01h | Bright Gamma offset (01h) |
| | 2nd | 46h | Red V1 Gamma |
| | 3rd | 46h | Green V1 Gamma |
| | 4th | 46h | Blue V1 Gamma |
| | 5th | 80h | Red V15 Gamma |
| | 6th | 80h | Green V15 Gamma |
| | 7th | 80h | Blue V15 Gamma |
| | 8th | 80h | Red V35 Gamma |
| | 9th | 80h | Green V35 Gamma |
| | 10th | 80h | Blue V35 Gamma |
| | 11th | 80h | Red V59 Gamma |
| | 12th | 80h | Green V59 Gamma |
| | 13th | 80h | Blue V59 Gamma |
| | 14th | 80h | Red V87 Gamma |
| | 15th | 80h | Green V87 Gamma |
| | 16th | 80h | Blue V87 Gamma |
| | 17th | 80h | Red V171 Gamma |
| | 18th | 80h | Green V171 Gamma |
| | 19th | 80h | Blue V171 Gamma |
| | 20th | 00h | Red V255 Gamma |
| | 21th | BEh | Red V255 Gamma |
| | 22th | 00h | Green V255 Gamma |
| | 23th | BEh | Green V255 Gamma |
| | 24th | 00h | Blue V255 Gamma |
| | 25th | BEh | Blue V255 Gamma |

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2) Gamma / LTPS Set Update

| Command | Parameter | | Description |
|---|---|---|---|
| F7h | 1st | 03h | Gamma + LTPS set update enable |

## [4] ETC Condition Set

| Command | Parameter | |
|---|---|---|
| F6h ( Source Control) | 1st | 00h |
| | 2nd | 02h |

| Command | Parameter | |
|---|---|---|
| B6h ( PenTile Control) | 1st | 0Ch |
| | 2nd | 02h |
| | 3rd | 03h |
| | 4th | 32h |
| | 5th | FFh |
| | 6th | 44h |
| | 7th | 44h |
| | 8th | C0h |
| | 9th | 00h |

| Command | Parameter | |
|---|---|---|
| D9h ( PenTile Control) | 1st | 14h |
| | 2nd | 40h |
| | 3rd | 0Ch |
| | 4th | CBh |
| | 5th | CEh |
| | 6th | 6Eh |
| | 7th | C4h |
| | 8th | 07h |
| | 9th | 40h |
| | 10th | 41h |
| | 11th | CBh |
| | 12th | 00h |
| | 13th | 60h |
| | 14th | 19h |

| Command | Parameter | |
|---|---|---|
| F4h ( Power Control ) | 1st | CFh |
| | 2nd | 0Ah |
| | 3rd | 12h |
| | 4th | 10h |
| | 5th | 1Eh |
| | 6th | 33h |
| | 7th | 02h |

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## [5] ELVSS Set

### 1) Power saving mode

| Command | Parameter | | Description |
|---|---|---|---|
| B1h | 1st | 04h | ID3 Value set |
| | 2nd | xxh | |

★ A9h> (ID3 Value) > 81h

### 2) Low temperature mode (Below 0℃ ) / Normal mode

| Command | Parameter | | Description |
|---|---|---|---|
| B1h | 1st | 04h | ELVSS : -4.4V |
| | 2nd | 95h | |

### Cf) DCDC-IC. STOD13AS Negative Output voltage levels

| Pulse | $V_{O2}$ | Pulse | $V_{O2}$ | Pulse | $V_{O2}$ | Pulse | $V_{O2}$ |
|---|---|---|---|---|---|---|---|
| 1 | -6.4 | 11 | -5.4 | 21 | -4.4 | 31 | -3.4 |
| 2 | -6.3 | 12 | -5.3 | 22 | -4.3 | 32 | -3.3 |
| 3 | -6.2 | 13 | -5.2 | 23 | -4.2 | 33 | -3.2 |
| 4 | -6.1 | 14 | -5.1 | 24 | -4.1 | 34 | -3.1 |
| 5 | -6.0 | 15 | -5.0 | 25 | -4.0 | 35 | -3.0 |
| 6 | -5.9 | 16 (*) | -4.9 | 26 | -3.9 | 36 | -2.9 |
| 7 | -5.8 | 17 | -4.8 | 27 | -3.8 | 37 | -2.8 |
| 8 | -5.7 | 18 | -4.7 | 28 | -3.7 | 38 | -2.7 |
| 9 | -5.6 | 19 | -4.6 | 29 | -3.6 | 39 | -2.6 |
| 10 | -5.5 | 20 | -4.5 | 30 | -3.5 | 40 | -2.5 |
| | | | | | | 41 | -2.4 |

(*) Default value

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## [6] ACL Set

1) ACL parameter setting ( @ Full white mode )

| CMD | Parameter | Luminance Cut ratio 50% | Description |
|---|---|---|---|
| C1h | 1st | 47h | Coefficient register of Red.(When RG1BG2 convert Y) |
| | 2nd | 53h | Coefficient register of Green.(When RG1BG2 convert Y) |
| | 3rd | 13h | Coefficient register of Blue.(When RG1BG2 convert Y) |
| | 4th | 53h | Coefficient register of Green 2.(When RG1BG2 convert Y) |
| | 5th | 00h | ACL window horizontal strat point register. |
| | 6th | 00h | ACL window horizontal strat point register. |
| | 7th | 02h | ACL window horizontal end point register. |
| | 8th | CFh | ACL window horizontal end point register. |
| | 9th | 00h | ACL window vertical strat point register. |
| | 10th | 00h | ACL window vertical strat point register. |
| | 11th | 04h | ACL window vertical strat end register. |
| | 12th | FFh | ACL window vertical strat end register. |
| | 13th | 00h | Delta Y register for inflection point 0.(Y avrage = 15) |
| | 14th | 00h | Delta Y register for inflection point 1.(Y avrage = 31) |
| | 15th | 00h | Delta Y register for inflection point 2.(Y avrage = 47) |
| | 16th | 00h | Delta Y register for inflection point 3.(Y avrage = 63) |
| | 17th | 00h | Delta Y register for inflection point 4.(Y avrage = 79) |
| | 18th | 01h | Delta Y register for inflection point 5.(Y avrage = 95) |
| | 19th | 09h | Delta Y register for inflection point 6.(Y avrage = 111) |
| | 20th | 10h | Delta Y register for inflection point 7.(Y avrage = 127) |
| | 21st | 18h | Delta Y register for inflection point 8.(Y avrage = 143) |
| | 22nd | 1Fh | Delta Y register for inflection point 9.(Y avrage = 159) |
| | 23rd | 27h | Delta Y register for inflection point 10.(Y avrage = 175) |
| | 24th | 2Eh | Delta Y register for inflection point 11.(Y avrage = 191) |
| | 25th | 36h | Delta Y register for inflection point 12.(Y avrage = 207) |
| | 26th | 3Dh | Delta Y register for inflection point 13.(Y avrage = 223) |
| | 27th | 45h | Delta Y register for inflection point 14.(Y avrage = 239) |
| | 28th | 4Ch | Delta Y register for inflection point 15.(Y avrage = 255) |

2)ACL On/Off command

| Command | Parameter | | Description |
|---|---|---|---|
| C0h | 1st | **h | - 00h : ACL Off (default)<br>- 01h : ACL On |

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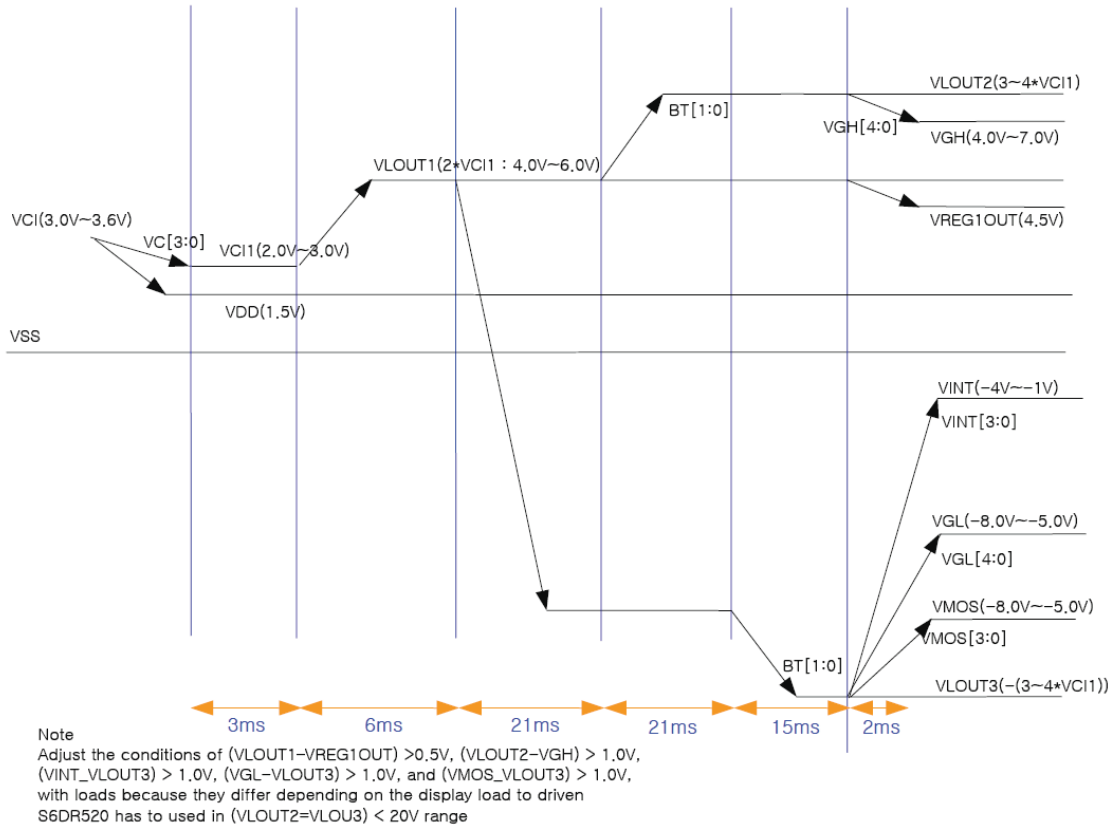
## 9-2. Internal Power Supply Pattern Diagram




Note
Adjust the conditions of (VLOUT1-VREG1OUT) >0.5V, (VLOUT2-VGH) > 1.0V,
(VINT_VLOUT3) > 1.0V, (VGL-VLOUT3) > 1.0V, and (VMOS_VLOUT3) > 1.0V,
with loads because they differ depending on the display load to driven
S6DR520 has to used in (VLOUT2=VLOU3) < 20V range

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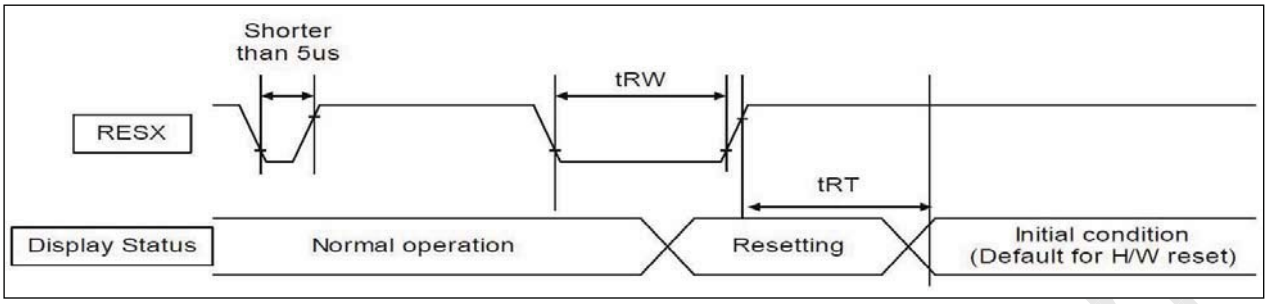
# 10. AC characteristics

## 10-1. Reset Timing




| Signal | Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|---|
| RESX | tRW | Reset pulse duration | 10 | – | µs |
| | tRT | Reset cancel | – | 5(5) | ms |
| | | | – | 120(6, 7) | |

NOTE:

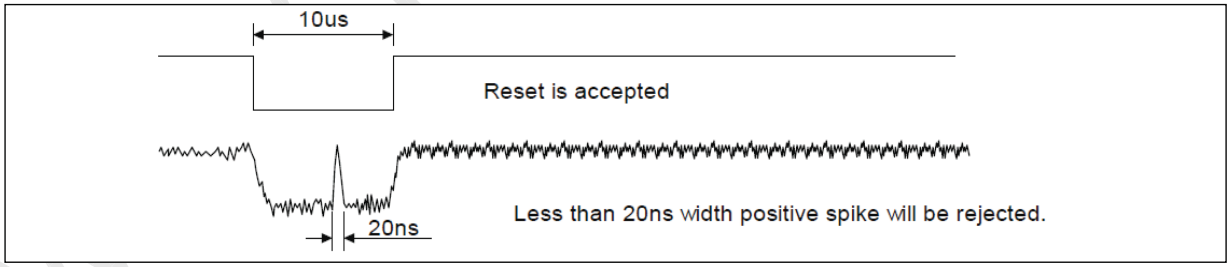
1. The reset cancel includes also required time for loading ID bytes (or similar) from EEPROM (or similar) to ID (or similar) registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table below

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset rejected |
| Longer than 10µs | Reset |
| Between 5µs and 9µs | Reset starts |

3. During the Resetting period, the display will be blanked (The display enters blanking sequence, in which maximum time is 120ms, when Reset Starts in Sleep Outmode. The display remains in the blank state at Sleep In mode) and then return to default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:




5. When Reset is applied during sleep In Mode.

6. When Reset is applied during Sleep out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also sleep out command cannot be sent out for 120msec.

8. HW reset cannot cause any spike/glitch on control or data lines or spike/glitch/noise on power (VCI and VDD3) lines.

9. The display module can also initialize and calibrate DSI-CLK± DSI-D0± and DSI-D1± lanes within 5ms if it is needed when DSI has been selected to use.

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# 11. MIPI characteristics

## 11-1. DC Characteristics

| Items | | Parameter | Min. | Nom. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| LP_TX | Thevenin output high level | VOH | 1.1 | 1.2 | 1.3 | V | |
| | Thevenin output low level | VOL | – 50 | – | 50 | mV | |
| | Output impedance of LP transmitter | ZOLP | 110 | – | – | Ω | (1) |
| HS_RX | Common-mode voltage HS receive mode | VCMRX (DC) | 70 | – | 330 | mV | (2) (3) |
| | Differential input high threshold | VIDTH | – | – | 70 | | |
| | Differential input low threshold | VIDTL | – 70 | – | – | | |
| | Single-ended input high voltage | VIHHS | – | – | 460 | | (2) |
| | Single-ended input low voltage | VILHS | – 40 | – | – | | |
| | Single-ended threshold for HS termination enable | VTERM-EN | – | – | 450 | | |
| | Differential input impedance | ZID | 80 | 100 | 125 | Ω | |
| LP_RX | Logic1 input voltage | VIH | 880 | – | – | mV | |
| | Logic0 input voltage, not in ULP State | VIL | – | – | 550 | | |
| | Input hysteresis | VHYST | 25 | – | – | | (4) |
| LP_CD | Logic1 contention threshold | VIHCD | 450 | – | – | | |
| | Logic0 contention threshold | VIOLED | – | – | 200 | | |

**NOTE:**

1. Even though a maximum value for ZOLP is not specified, the output impedance of the LP transmitter ensures that the TRLP/TFLP specification is met
2. Excluding additional RF interference of 100mV peak sine wave beyond 450MHz.
3. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz
4. Temperature condition 25°C

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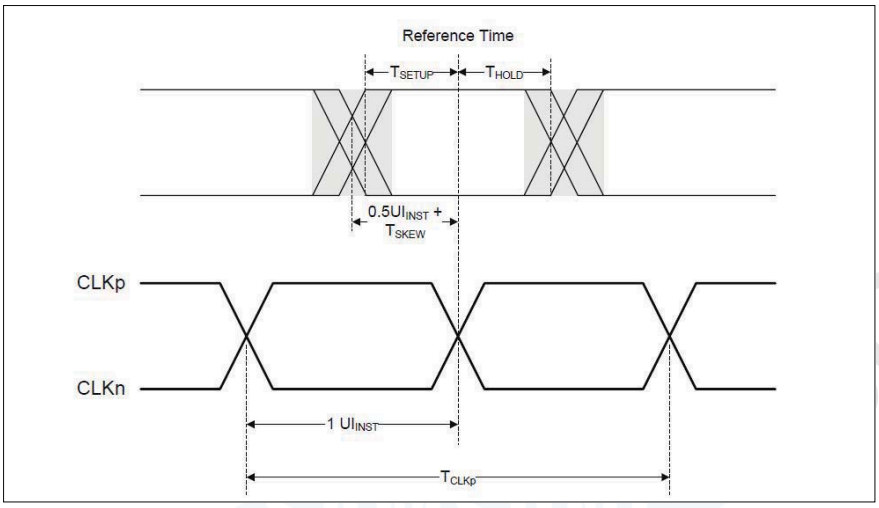
## 11-2. High Speed Data-clock Timing

Host sends a differential clock signal to the **S6E8AA001** to be used for data sampling. This signal is a DDR (Half-rate) clock and has one transition per data bit time. The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure below.




| Clock Parameter | Symbol | # of d-lane | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| UI instantaneous | UIINST | 4 | 2 | | 12.5 | ns | (1, 2) |

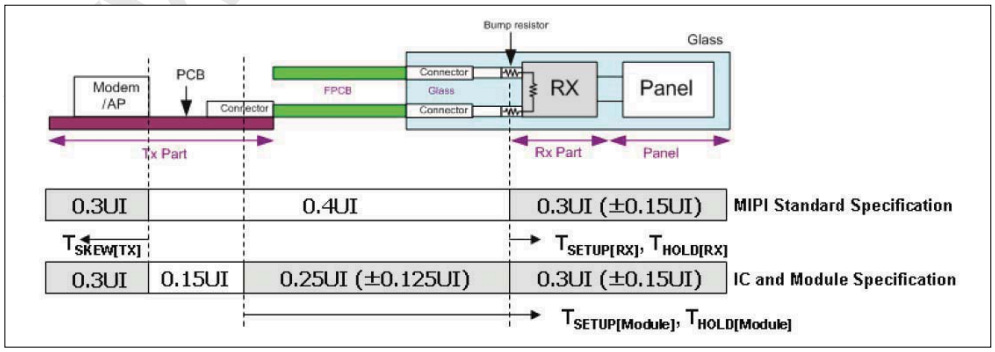
**NOTE:**

1. This value corresponds to a minimum 80Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Data to clock skew (Measured at transmitter) | TSKEW[TX] | – 0.15 | – | 0.15 | UIINST | (1) |
| Data to clock setup time (Receiver) | TSETUP[RX] | 0.15 | – | – | UIINST | (2) |
| Clock to data hold time (Receiver) | THOLD[RX] | 0.15 | – | – | UIINST | |

**NOTE:**

1. Total silicon and package delay budget of 0.3 × UIINST
2. Total setup and hold window for receiver of 0.3 × UIINST
3. TSETUP[RX] and THOLD[RX] are only for RX without FPCB and connector and guaranteed by design. For module test, TSETUP[Module] and THOLD[Module] specification including FPCB and connector is 0.275UIINST. Refer to Figure below.




MIPI data-clock timing specifications on Module

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# 12. Interface

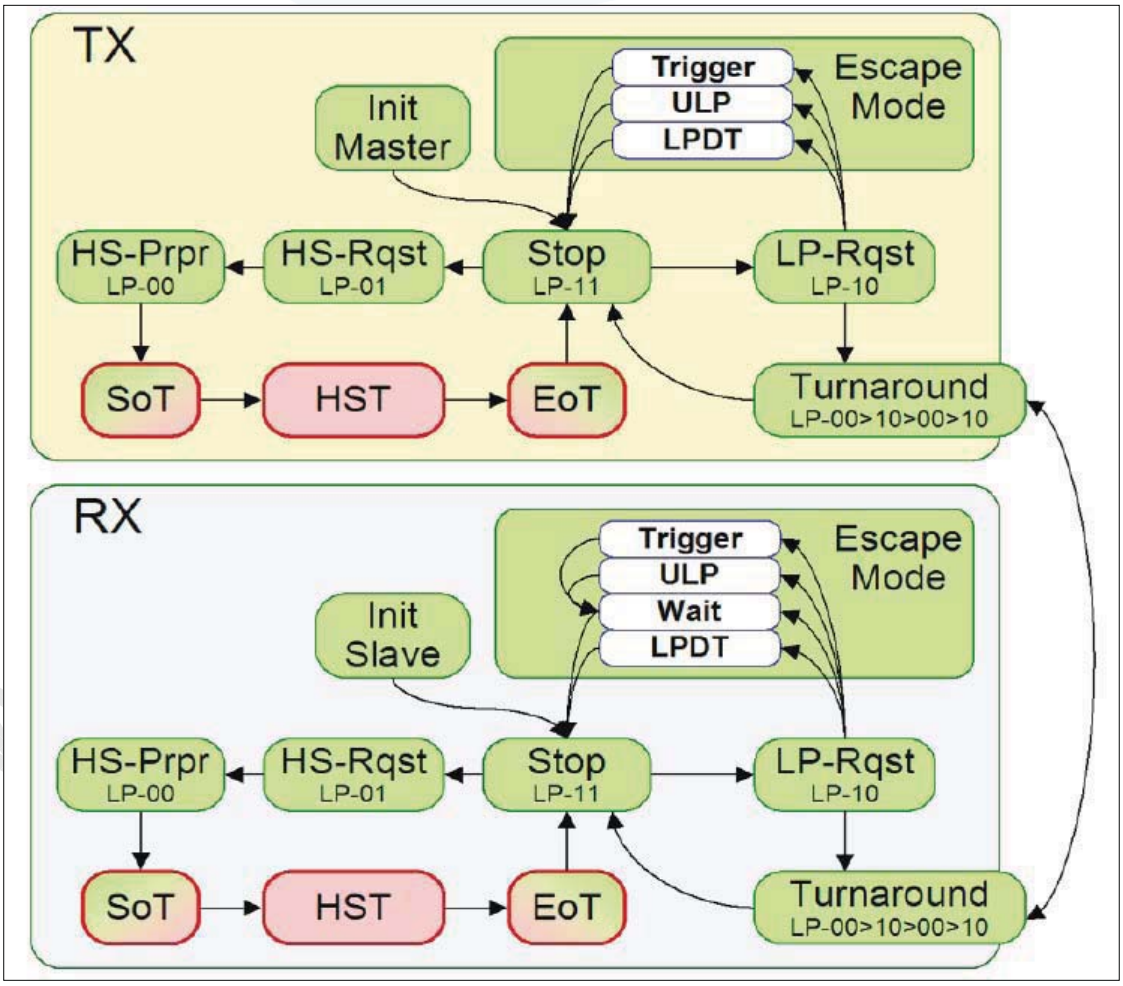
## 12-1. Feature

- ☐ 2/4 data lanes
- ☐ HS (High speed) transmission (Unidirectional)
- ☐ LP (Low power) transmission (Bidirectional)
- ☐ Both video and command modes are supported
- ☐ Diagnostic function-checksum and ECC error monitoring
- ☐ Functionality supported by Escape mode
- ☐ Clock lane supports ULPS
- ☐ Packet-based protocol

## 12-2 MIPI D-PHY

### 12-2-1. Global Operation

Figure below shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround and Initialization

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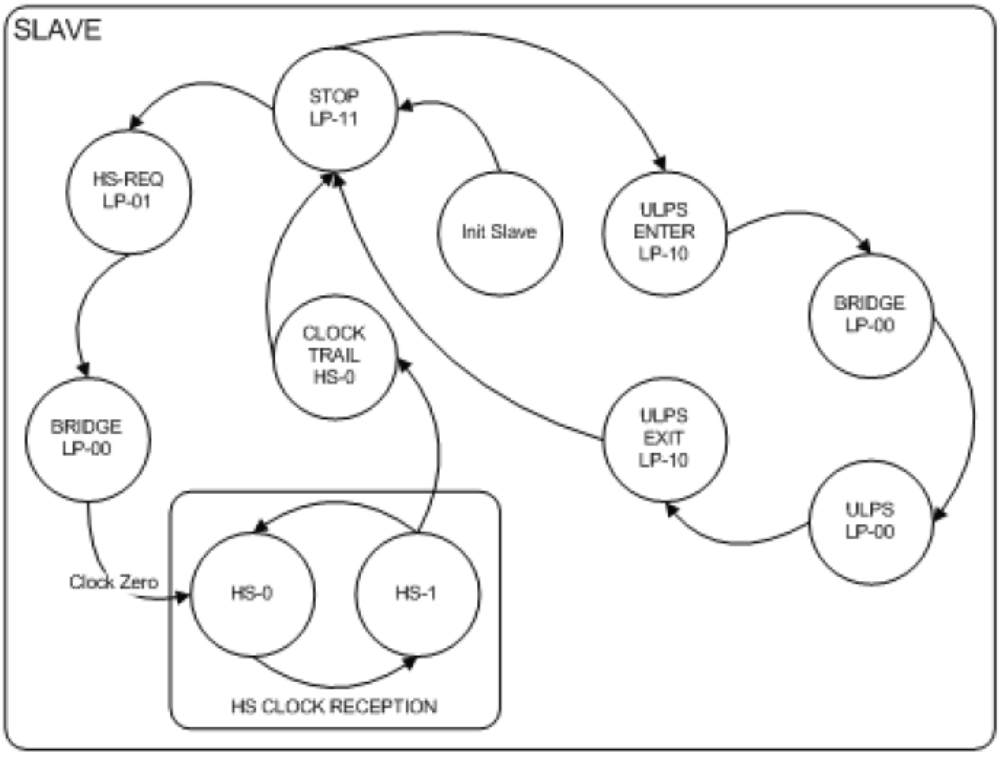
### 12-2-2. Lane state

| State Code | Line Voltage Levels | | High-speed | Low-power | |
|---|---|---|---|---|---|
| | DP-line | DN-line | Burst Mode | Control Mode | Escape Mode |
| HS-0 | HS low | HS high | Differential-0 | N/A | N/A |
| HS-1 | HS high | HS low | Differential-1 | N/A | N/A |
| LP-00 | LP low | LP low | N/A | Bridge | Space |
| LP-01 | LP low | LP high | N/A | HS-Rqst | Mark-0 |
| LP-10 | LP high | LP low | N/A | LP-Rqst | Mark-1 |
| LP-11 | LP high | LP high | N/A | Stop | N/A |

### 12-2-3. Clock Lane Flow Diagram

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### 12-2-4. High Speed Data Transmission

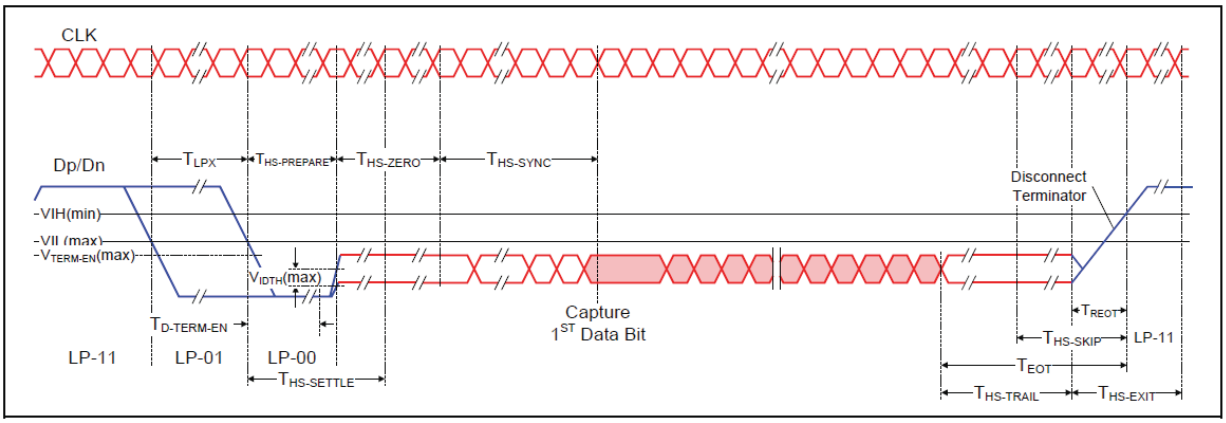
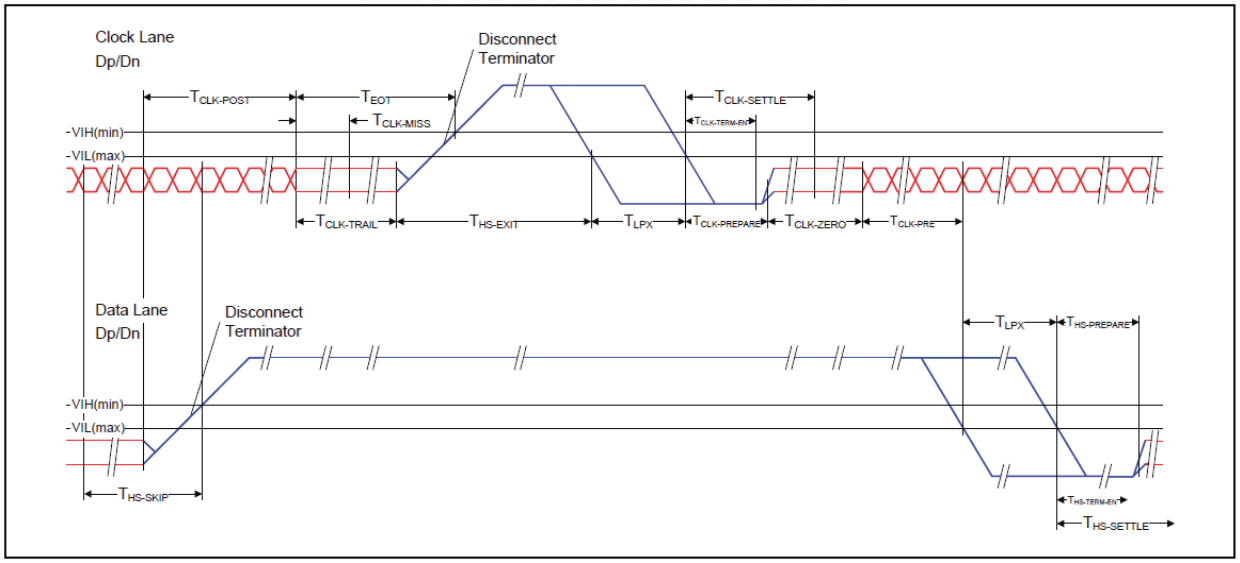



Figure shows the sequence of the high speed data transmission including SoT data.

### 12-2-5. High Speed Clock Transmission




This Figure shows the sequence of the high speed clock transmission. In high speed mode the clock lane provides a low-swing differential DDR clock signal from Master to Slave for high speed data transmission.



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### 12-2-6. Escape Mode

Escape Mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Though Escape Mode operation is optional in D-PHY, the host processor and peripheral in which Command Mode operation is supported shall implement reverse-direction Escape Mode as well as forward direction Escape Mode.

A Data Lane shall enter Escape Mode via an Escape Mode Entry procedure (LP-11,LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape Mode in Space state (LP-00). If an LP-10 is detected after the first Bridge state or an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape Mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

Once Escape Mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Table below (MIPI Escape Mode Entry Code) lists all currently available Escape Mode commands and actions. All unassigned commands are reserved for future expansion

| Escape Mode Action | Command Type | Entry Command Pattern (First Bit Transmitted to Last Bit Transmitted) | S6E8AA0 | |
|---|---|---|---|---|
| | | | LP-RX | LP-TX |
| Low-power data transmission | Mode | 11100001 | O | O |
| Ultra-low power state | Mode | 00011110 | O | – |
| Undefined-1 | Mode | 10011111 | – | – |
| Undefined-2 | Mode | 11011110 | – | – |
| Reset-trigger (Remote application) | Trigger | 01100010 | O | – |
| Unknown-3 | Trigger | 01011101 | – | - |
| Unknown-4 (Acknowledge trigger) | Trigger | 00100001 | – | O |
| Unknown-5 | Trigger | 10100000 | – | – |

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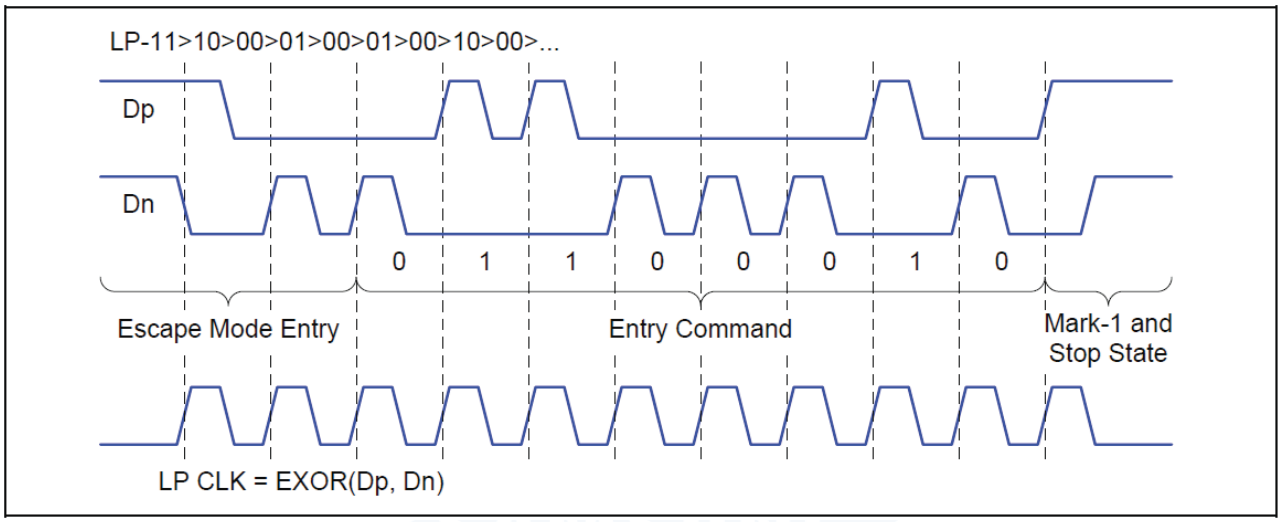
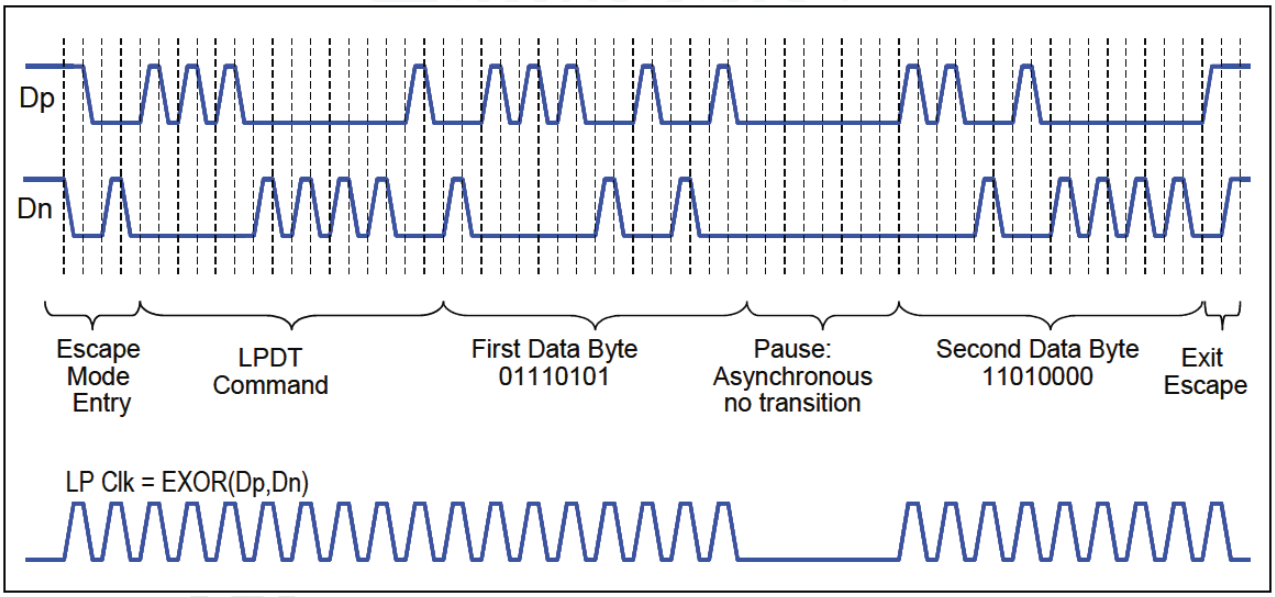
### 12-2-7. Low Power Data Lane Operation

The Figure below shows the sequence of the low power data transmission. The Escape mode uses the spaced one hot bit encoding for asynchronous communication.

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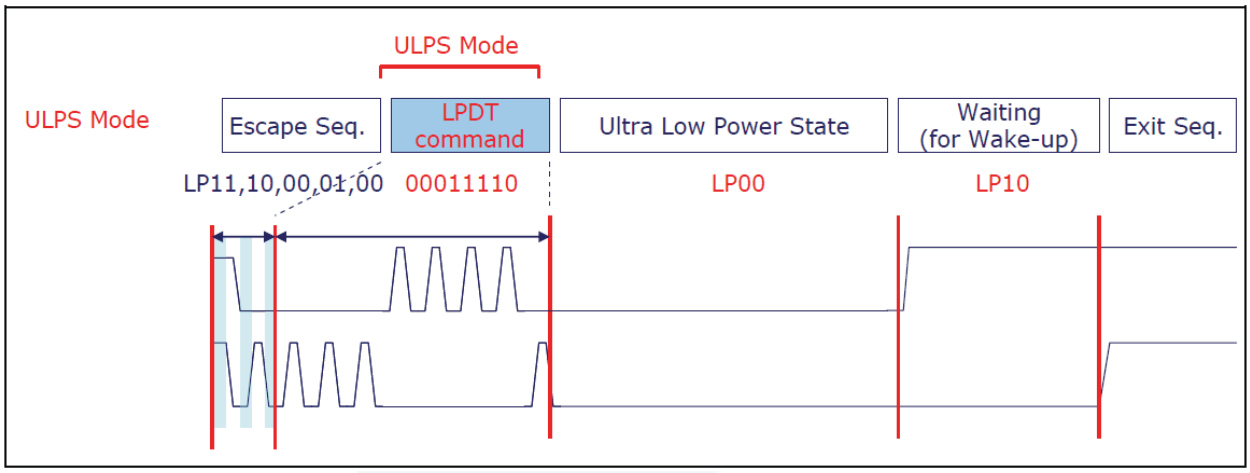
### 12-2-8. Ultra-low Power State

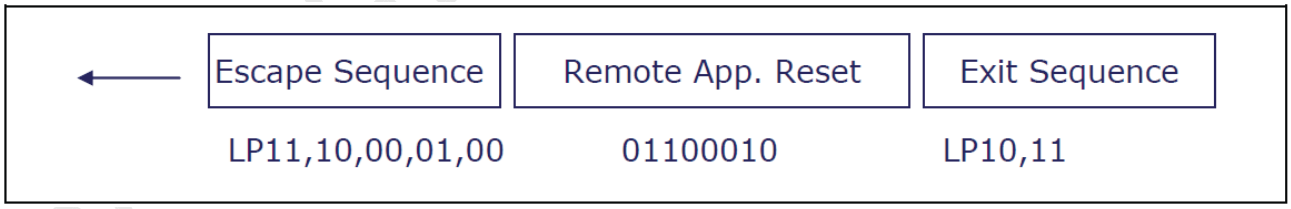
If the Ultra Low Power Entry Command is sent after an Escape Mode Entry command, the Lane shall enter the Ultra Low Power State (ULP). This Command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop State. Figure below shows an Ultra Low Power Entry and Exit example.




The Host processor provides LP10 state before Exit to wait for the MIPI SLAVE's stabilization. ULPS packet turn off the PHY_IO HS_RX. The ULPS turn off the bias current of HS_RX. The LP10 wakeup state is a trigger to turn on the HS_RX before normal STOP state.

### 12-1-9. Remote Application Reset

Remote Application Reset Command is used in case of transmission from the host processor to the peripheral. If the Entry Command Pattern matches the Remote Application Reset Command a Trigger is flagged to the protocol at the peripheral side via the logical PPI.
Figure below shows MIPI remote application reset packet using LP mode. The host processor can send software reset trigger by Remote Application Reset Packet.

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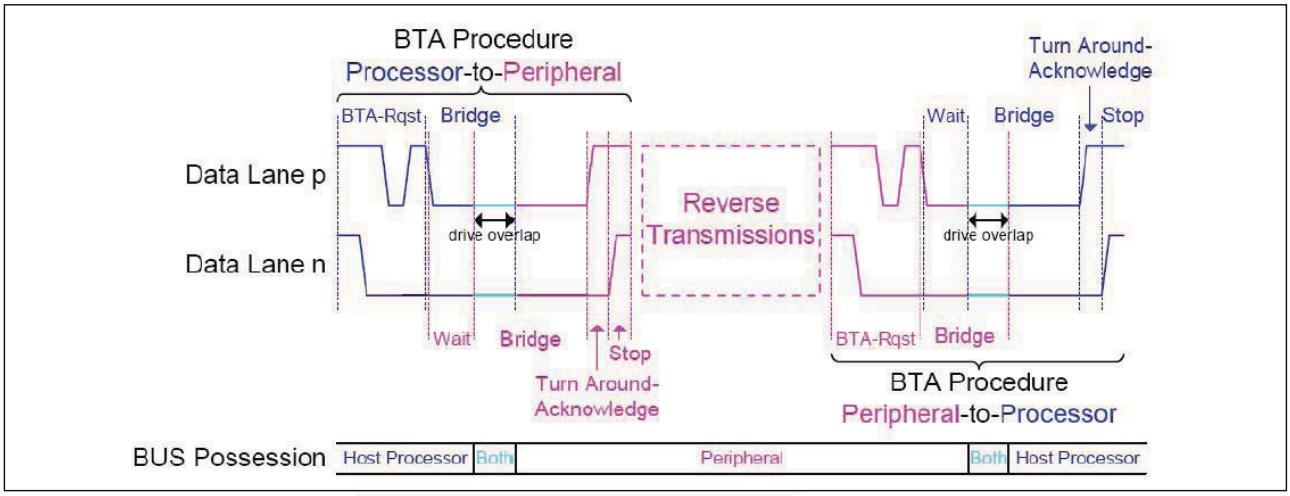
### 12-2-10. Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Figure below shows the BTA procedure graphically.




The low power clock timing for both sides of the Link does not have to be the same, but may differ. However, the ratio between the Low Power State Periods, $T_{LPX}$ is constrained to ensure proper Turnaround behavior. The $T_{LPX}$ (Master)/ $T_{LPX}$ (Slave) shall be between 2/3 (0.667) and 3/2 (1.50). The handshake process for BTA allows only limited mismatch of Escape Mode clock frequencies between a host processor and a peripheral.

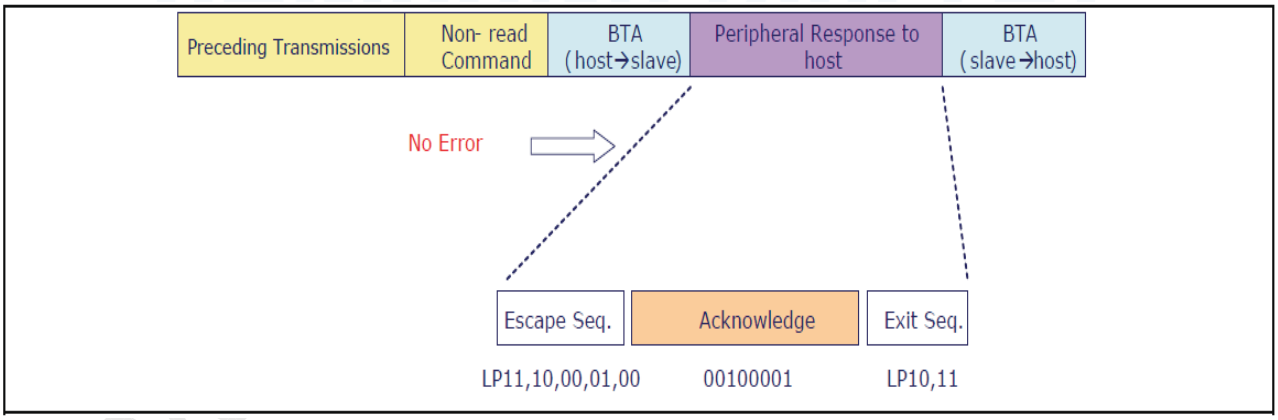



Figure shows an example of BTA after non-read command. The SLAVE get the lane controllability by BTA procedure to send the acknowledge packet on the successful data reception.

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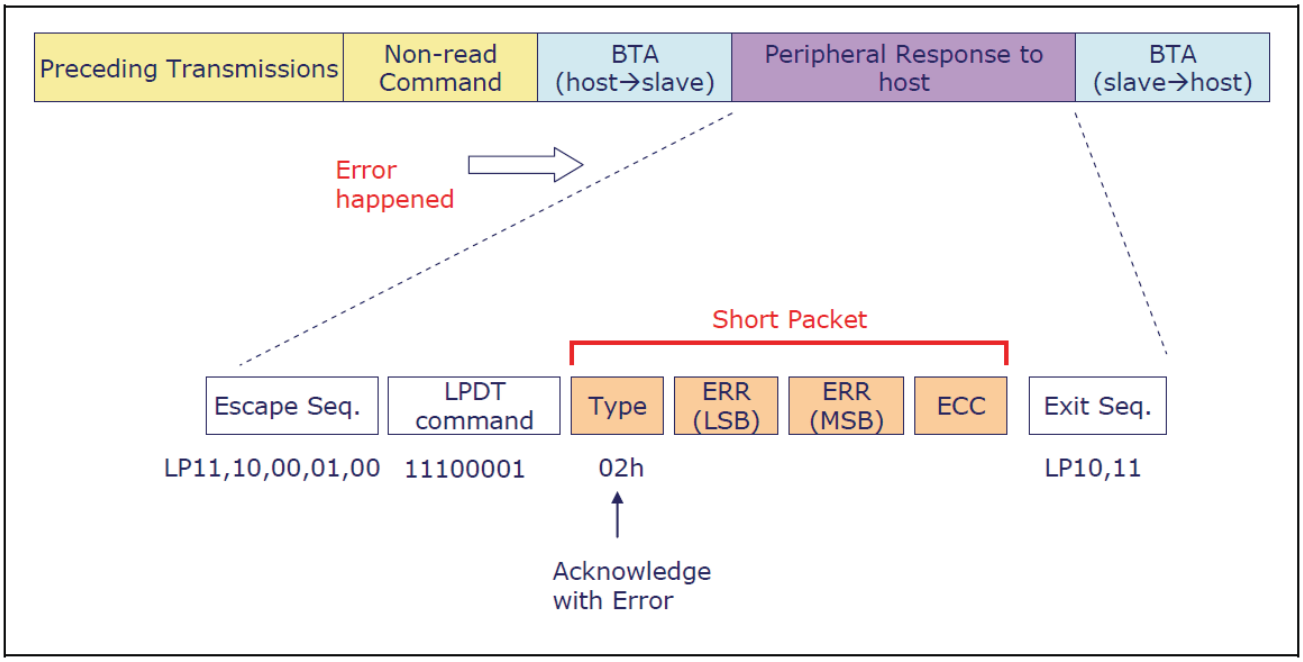


Figure shows an example of BTA after non-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknowledge with error packet on the data reception error.

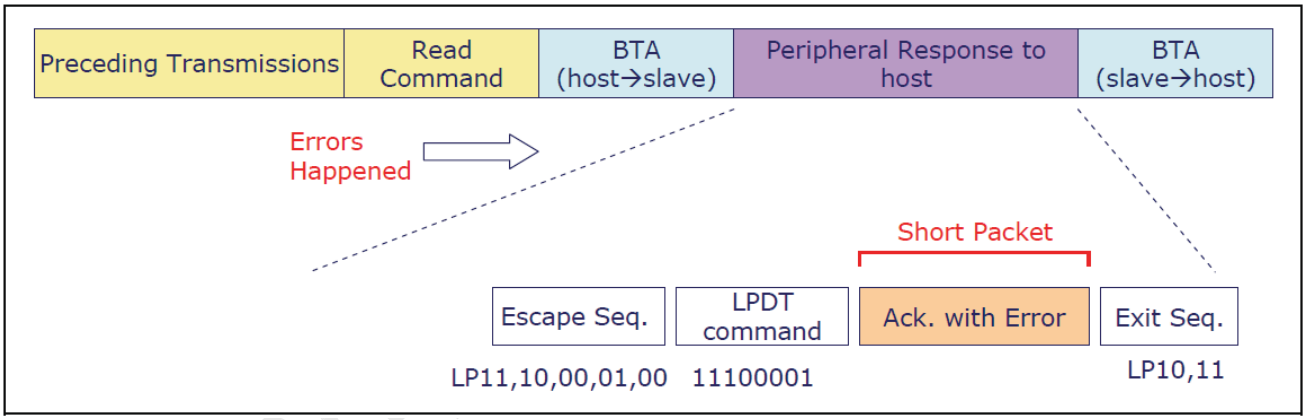


Figure shows an example of BTA after-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknowledge with error packet on the data reception error.

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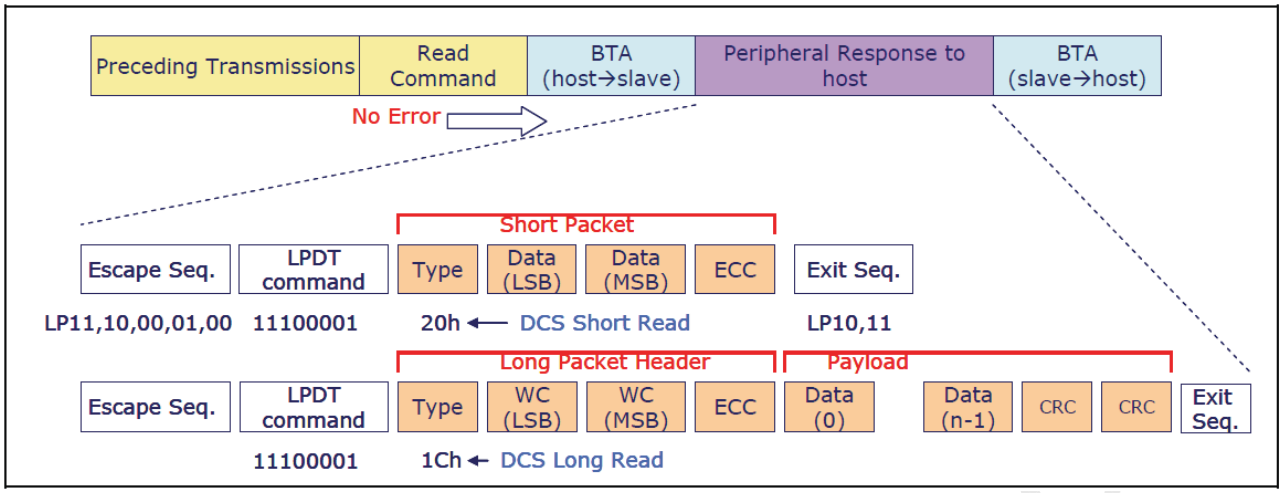


Figure shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet on the successful data reception.

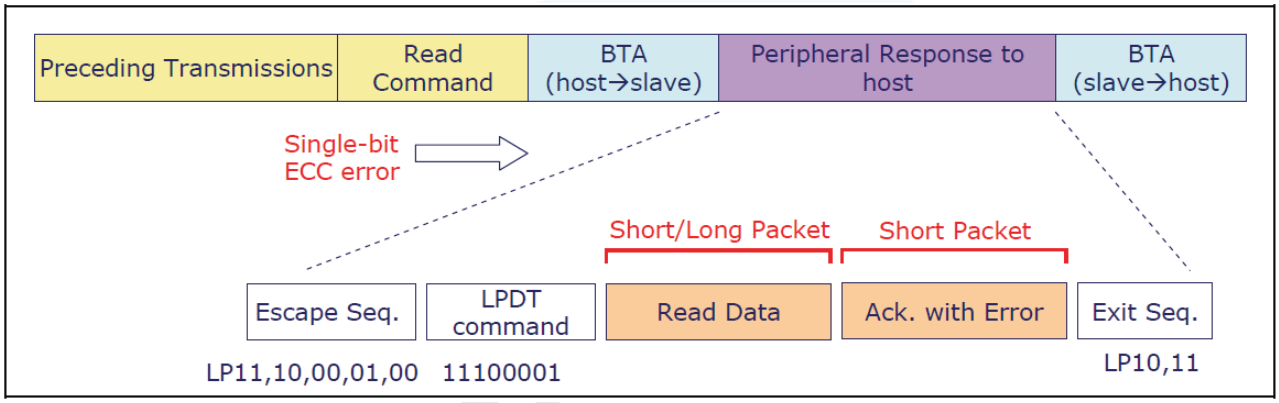


Figure shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet and acknowledge with error on the one bit error.

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### 12-2-11. Global Operation Timings

The values in the table require a clock tolerance no worse than ± 10% for implementation.

| Parameter | Description | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| $T_{CLK-MISS}$ | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX. | | | 60 | ns | (1, 6) |
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$. | 60ns + 52 × UI | | | | |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI | (5) |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns | |
| $T_{CLK-SETTLE}$ | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$. | 95 | | 300 | | (6) |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX.}$ | Time for Dn to reach $V_{TERM-EN}$ | | 38 | | |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | | (5) |
| $TC_{LK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | | |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX.}$ | Time for Dn to reach $V_{TERM-EN}$ | | 35ns + 4 × UI | | (6) |
| $T_{EOT}$ | Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst. | | | 105ns + n × 12 × UI | | (3, 5) |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | | | ns | (5) |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40ns + 4 × UI | | 85ns + 6 × UI | | |

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| Parameter | Description | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145ns + 10 × UI | | | | |
| $T_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. | 85ns + 6 × UI | | 145ns + 10 × UI | | (6) |
| $T_{HS-SKIP}$ | Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst. | 40 | | 55ns + 4 × UI | | |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | Max (n × 8 × UI, 60ns + n × 4 × UI) | | | | (2, 3, 5) |
| $T_{INIT}$ | | | | | | |
| $T_{LPX}$ | Transmitted length of any Low-Power state period | 56.25 | 62.5 | 68.75 | ns | (4, 5) |
| Ratio $T_{LPX}$ | Ratio of $T_{LPX}$(MASTER)/$T_{LPX}$(SLAVE) between Master and Slave side | 2/3 | | 3/2 | | |
| $T_{TA-GET}$ | Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | 5 × $T_{LPX}$ | | | ns | (5) |
| $T_{TA-GO}$ | Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | 4 × $T_{LPX}$ | | | | |
| $T_{TA-SURE}$ | Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX}$ | | 2 × $T_{LPX}$ | | |
| $T_{WAKEUP}$ | Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS. | 1 | | | ms | |

NOTE:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If a > b then max (a, b) = a otherwise max (a, b) = b
3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
4. $T_{LPX}$ is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter
6. Receiver-specific parameter

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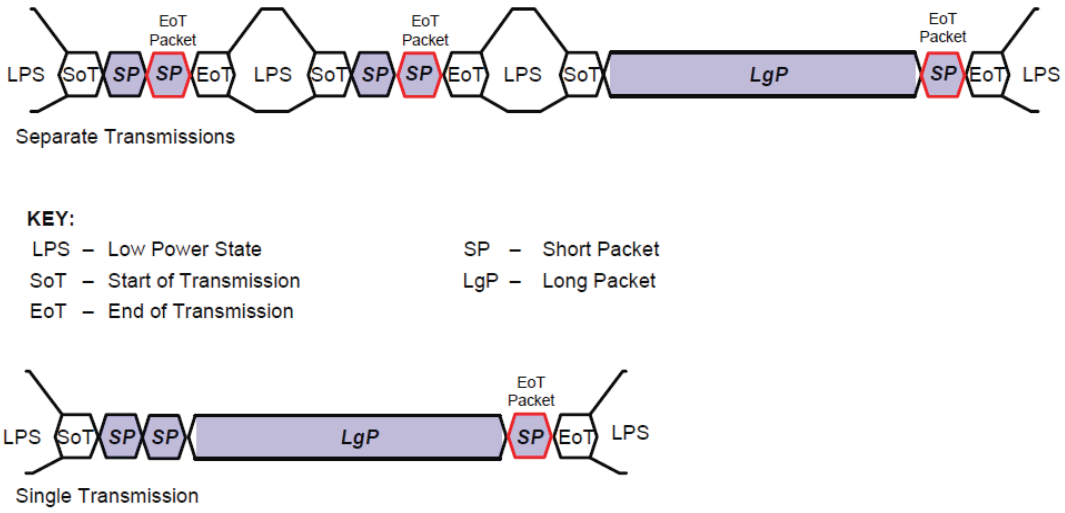
## 12-3 MIPI DSI

### 12-3-1. Multiple Packets Per Transmission

The MIPI CORE of S6E8AA0 supports four data transmission defined in MIPI DSI specification. And in order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp packet can be enabled or disabled with register.




### 12-3-2. General Packet Structure

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet.

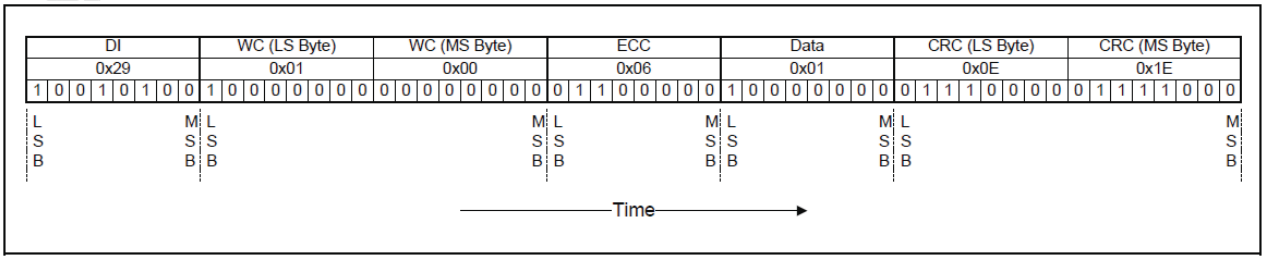
### 12-3-3. Common Packet Element

Long and Short packets have several common elements

### 12-3-4. Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Figure below shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

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### 12-3-5. Data Type Command Table

| Data Type, | | Description | Packet Size | (VD_PKT,GN_PKT) | | | |
|---|---|---|---|---|---|---|---|
| (hex) | (binary) | | | LL | HL | LH | HH |
| 01h | 00 0001 | Sync event, V sync start | Short | | O | | O |
| 11h | 01 0001 | Sync event, V sync end | Short | | O | | O |
| 21h | 10 0001 | Sync event, H sync start | Short | | O | | O |
| 31h | 11 0001 | Sync event, H sync end | Short | | O | | O |
| 08h | 00 1000 | End of transmission packet | Short | O | O | O | O |
| 02h | 00 0010 | Color mode (CM) off command | Short | | O | | O |
| 12h | 01 0010 | Color mode (CM) on command | Short | | O | | O |
| 22h | 10 0010 | Shut down peripheral command | Short | | O | | O |
| 32h | 11 0010 | Turn on peripheral command | Short | | O | | O |
| 03h | 00 0011 | Generic short WRITE, no parameters | Short | | | - | - |
| 13h | 01 0011 | Generic short WRITE, 1parameter | Short | | | O | O |
| 23h | 10 0011 | Generic short WRITE, 2parameters | Short | | | - | - |
| 04h | 00 0100 | Generic READ, no parameters | Short | | | - | - |
| 14h | 01 0100 | Generic READ, 1parameter | Short | | | O | O |
| 24h | 10 0100 | Generic READ, 2parameters | Short | | | - | - |
| 05h | 00 0101 | DCS WRITE, no parameters | Short | O | O | O | O |
| 15h | 01 0101 | DCS WRITE, 1parameter | Short | O | O | O | O |
| 06h | 00 0110 | DCS READ, no parameters | Short | O | O | O | O |
| 37h | 11 0111 | Set maximum return packet size | Short | O | O | O | O |
| 09h | 00 1001 | Null packet, no data | Long | O | O | O | O |
| 19h | 01 1001 | Blanking packet, no data | Long | | O | | O |
| 29h | 10 1001 | Generic long write | Long | | | O | O |
| 39h | 11 1001 | DCS long write/write_LUT command packet | Long | O | O | O | O |
| 0Eh | 00_1110 | Packet pixel stream, 16bit RGB 565 format | Long | | O | | O |
| 1Eh | 01_1110 | Packet pixel stream, 18bit RGB 666 format | Long | | O | | O |
| 2Eh | 10_1110 | Packet pixel stream, 18bit RGB loosely 666 format | Long | | O | | O |
| 3Eh | 11 1110 | Packed pixel stream, 24-bit RGB, 888 format | Long | | O | | O |
| x0h&Fh | xx 0000 | DO NOT USE | | | | | |
| | xx 1111 | All unspecified codes are reserved | | | | | |

Note that VDT_PKT(H=Video & Command mode supported, L=Only Command mode) and GN_PKT(H=DCS & Generic supported, L=Only DCS).

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Data Types for Peripheral-sourced Packets

| Data Type (hex) | Data Type (binary) | Description | Packet Size | GN PKT | |
|---|---|---|---|---|---|
| | | | | L | H |
| 00h ~ 01h | 00 000x | Reserved | Short | – | – |
| 02h | 00 0010 | Acknowledge with error report | Short | O | O |
| 03h ~ 07h | 00 0011 ~ 00 0111 | Reserved | | – | – |
| 08h | 00 1000 | End of transmission Packet | Short | | |
| 09h ~ 10h | 00 1001 ~ 01 0000 | Reserved | | | |
| 11h | 01 0001 | Generic short READ response, 1-byte returned | Short | | O |
| 12h | 01 0010 | Generic short READ response, 2-bytes returned | Short | | O |
| 13h ~ 18h | 01 0011 ~ 01 1000 | Reserved | | – | – |
| 1Ah | 01 1010 | Generic long READ response | Long | | O |
| 1Bh | 01 1011 | Reserved | | – | – |
| 1Ch | 01 1100 | DCS long READ response | Long | O | O |
| 1Dh ~ 20h | 01 1101 ~ 10 0000 | Reserved | | – | – |
| 21h | 10 0001 | DCS short READ response, 1-byte returned | Short | O | O |
| 22h | 10 0010 | DCS short READ response, 2-bytes returned | Short | O | O |
| 23h ~ 28h | 10 0011 ~ 10 1000 | Reserved | | – | – |
| 29h ~ 3Fh | 10 1001 ~ 11 1111 | Reserved | | – | – |

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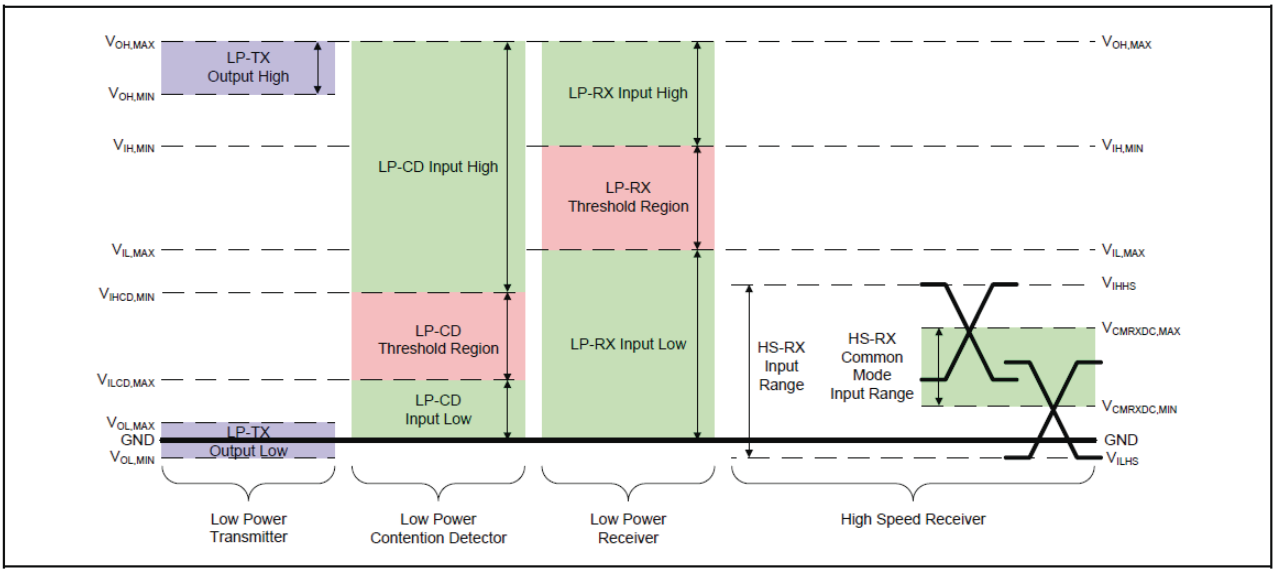
### 12-3-6. Error Report Packet

| Bit | Description | Implementation |
|---|---|---|
| 0 | SoT error | O |
| 1 | SoT sync error | O |
| 2 | EoT sync error | O |
| 3 | Escape mode entry command error | O |
| 4 | Low-power transmit sync error | O |
| 5 | HS receive timeout error (Timeout error) | O |
| 6 | False control error | O |
| 7 | Contention Detection error | O |
| 8 | ECC Error, single-bit (Detected and corrected) | O |
| 9 | ECC Error, multi-bit (Detected, not corrected) | O |
| 10 | Checksum error (Long packet only) | O |
| 11 | DSI data type not recognized | O |
| 12 | DSI VC ID invalid | O |
| 13 | Invalid transmission length | O |
| 14 | Reserved | – |
| 15 | DSI protocol violation | O |

### 12-3-7. Lane Connection Detection




The Low-power receiver and a separate contention detector shall be used in a bi-directional Data Lane to monitor the line voltage on each Low-power signal. The Low-power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than $V_{IL}$. The contention detector shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than $V_{IHCD}$. An LP low fault shall not be detected when the pin voltage is less than $V_{ILCD}$.

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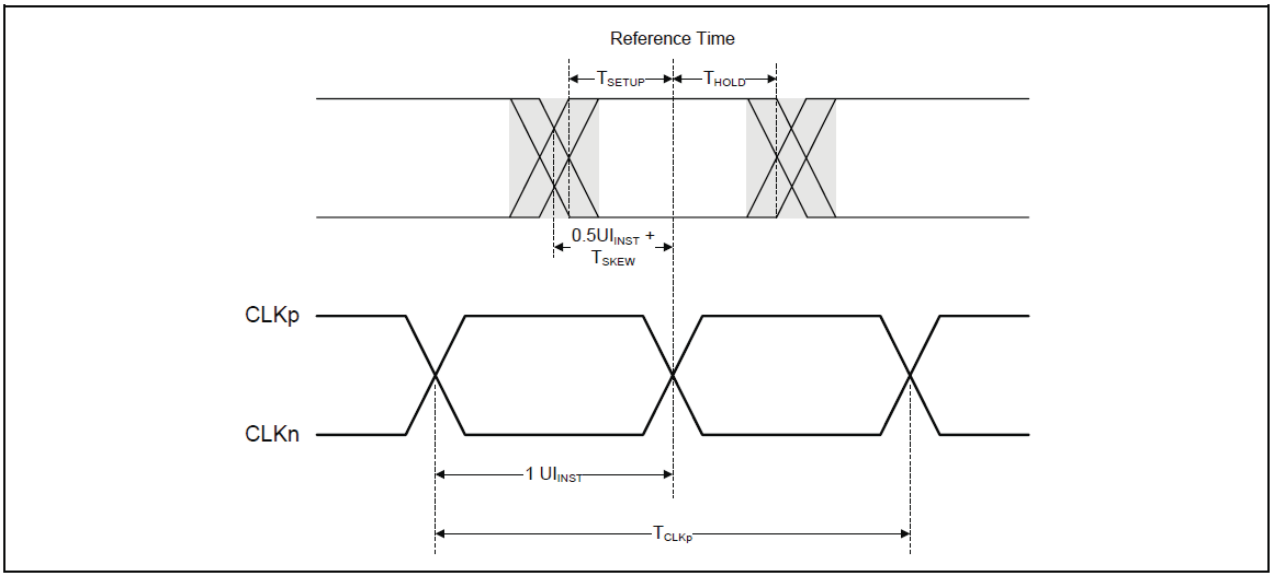
## 12-4 MIPI Characteristics

### 12-4-1. High Speed Data-clock Timing

Host sends a differential clock signal to the S6E8AA0 to be used for data sampling. This signal is a DDR (Half-rate) clock and has one transition per data bit time. The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in figure below.




| Clock Parameter | Symbol | # of d-lane | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| UI instantaneous | $UII_{NST}$ | 4 | 2 | | 12.5 | ns | (1,2) |

**NOTE:**

1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Data to Clock Skew (Measured at transmitter) | $T_{SKEW[TX]}$ | -0.15 | | 0.15 | UIINST | (1) |
| Data to Clock Setup Time (Receiver) | $T_{SETUP[RX]}$ | 0.15 | | | UIINST | (2) |
| Clock to Data Hold Time (Receiver) | $T_{HOLD[RX]}$ | 0.15 | | | UIINST | |

**NOTE:**

1. Total silicon and package delay budget of 0.3 × UIINST
2. Total setup and hold window for receiver of 0.3 × UIINST
3. TSETUP[RX] and THOLD[RX] are only for RX without FPCB and connector and guaranteed by design. For module test, TSETUP[Module] and THOLD[Module] specification including FPCB and connector is 0.275UIINST. Refer to figure below

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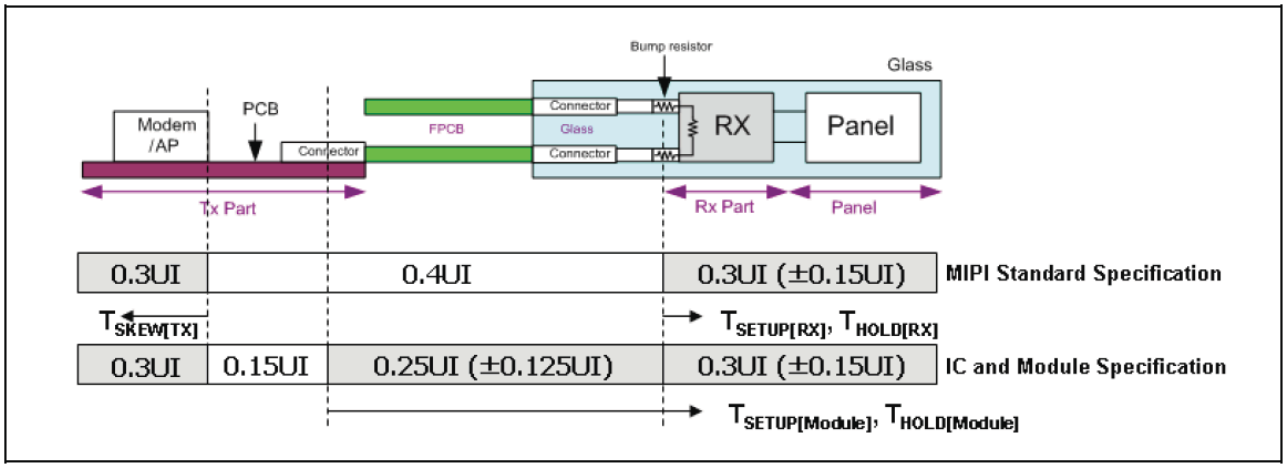


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# 13. Quality Level

## 13-1. AMOLED Module of Characteristic Inspection

### 13-1-1. The environmental conditions

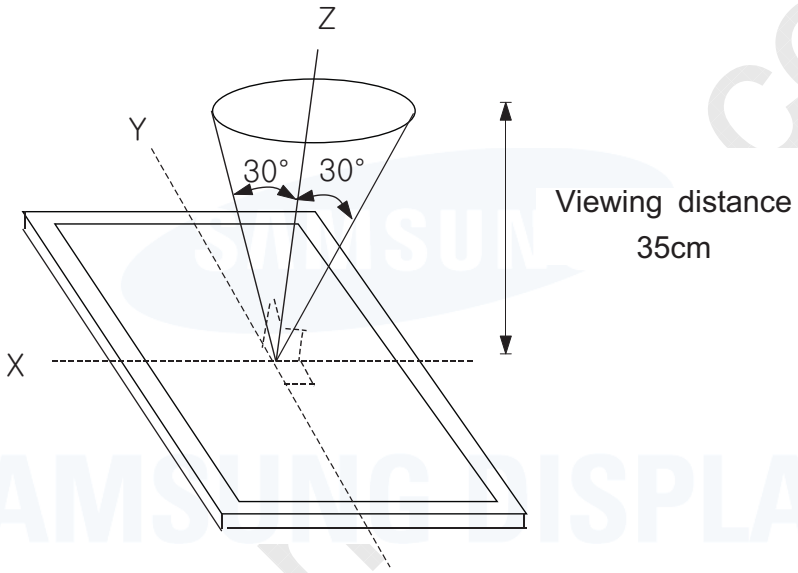
① Temperature & Humidity

Room temperature : 22 ± 3℃

Humidity : 65 ± 20%RH

② Viewing distance : 35cm ± 5cm

Viewing angle(tolerance) : ± 30°




③ Ambient light intensity : 800 ~ 1200 lux

### 13-1-2. Window

The environmental conditions for inspection shall be as follows.

① Light source : D65, Bar type 1 Lamp

② Ambient light intensity : 800 ~ 1200 lux

③ Viewing Distance : 35 ± 5cm

④ Viewing angle (tolerance) : the front side 90°(Z) ± 30°

⑤ Viewing Time : 10 ± 2 sec

⑥ Inspection Background : Only Black

⑦ Inspection Mode : Only Reflection inspection

⑧ Color variation: Transmitted inspection by backlight source (Light intensity : 400lux)

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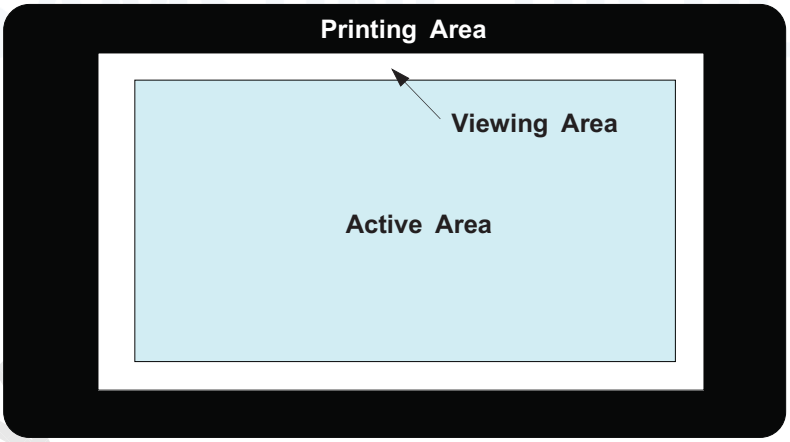
## 13-2. Sampling Procedures for each item's acceptance table

| Defect type | Sampling Procedures | AQL |
|---|---|---|
| Major Defect | MIL-STD-105D Inspection level Ⅰ<br>normal inspection<br>single sample inspection | 0.65 |
| Minor Defect | MIL-STD-105D Inspection level Ⅰ<br>normal inspection<br>single sample inspection | 1.5 |

① Major defect
: A major defect refers to a defect which may substantially degrade usability for product applications.

② Minor defect
: A minor defects refers to a defect which is not considered to substantially degrade product application,or a defect which deviates from existing standards almost unrelated to the effective use of the product or its operation.

③ Determination of inspection area : Active Area + Viewing Area
Defect in "Out of Viewing Area" Zone should not be judged.

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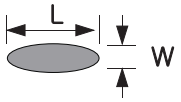
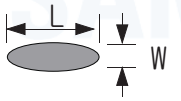
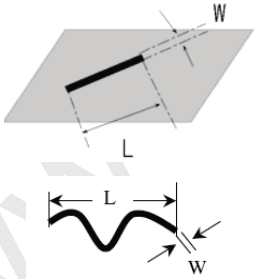
## 13-3. Inspection Item

### 13-3-1. Panel

<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>1</td><td>No Display</td><td>Not allowance</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular operating</td><td>Not allowance</td><td>Major</td></tr>
<tr><td>3</td><td>Dot Defect</td><td>
<table>
<tr><th colspan="2">Defect</th><th>Acceptable number</th></tr>
<tr><td colspan="2">Bright Dot</td><td>0</td></tr>
<tr><td rowspan="3">Dark Dot</td><td>Red</td><td>2</td></tr>
<tr><td>Green</td><td>2</td></tr>
<tr><td>Blue</td><td>2</td></tr>
<tr><td colspan="2">Total Acceptance Number</td><td>2</td></tr>
</table>
- Dark Dot Distance ≧ 20mm ( Acceptable )
</td><td>Minor</td></tr>
<tr><td>4</td><td>Polarizer<br>Dent / Bubble<br>  <br><br>Ø=(L+W)/2</td><td>
<table>
<tr><th>Size Ø (mm)</th><th>Acceptable number</th></tr>
<tr><td>Ø ≦ 0.20</td><td>Ignore</td></tr>
<tr><td>0.20 < Ø ≦ 0.50</td><td>3</td></tr>
<tr><td>0.50 < Ø ≦ 0.80</td><td>2</td></tr>
<tr><td>0.80 < Ø</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>5</td><td>Dark / Bright Spots<br>(Foreign Material)<br>  <br><br>Ø=(L+W)/2</td><td>
<table>
<tr><th>Size Ø (mm)</th><th>Acceptable number</th></tr>
<tr><td>Ø ≦ 0.15</td><td>Ignore</td></tr>
<tr><td>0.15 < Ø ≦ 0.25</td><td>2</td></tr>
<tr><td>0.25 < Ø</td><td>0</td></tr>
</table>
</td><td>Major</td></tr>
<tr><td>6</td><td>Polarizer Scratch / Fiber(Linear)<br>  <br></td><td>
<table>
<tr><th>Width (㎜)</th><th>Length (㎜)</th><th>Acceptable number</th></tr>
<tr><td>W ≦ 0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td rowspan="2">0.03 < W ≦ 0.05</td><td>L ≦ 2.0</td><td>Ignore</td></tr>
<tr><td>2.0 < L ≦ 5.0</td><td>2</td></tr>
<tr><td rowspan="2">0.05 < W ≦ 0.08</td><td>L ≦ 1.0</td><td>Ignore</td></tr>
<tr><td>1.0 < L ≦ 5.0</td><td>2</td></tr>
<tr><td>0.08 < W</td><td>-</td><td>0</td></tr>
</table>
</td><td>Major</td></tr>
<tr><td>7</td><td>Discoloration / Panel Stain</td><td>Ignore<br>If its limit sample is needed, it can be fixed mutually with a customer.</td><td>Major</td></tr>
<tr><td>8</td><td>WAD<br>(White angular dependency)</td><td>Ignore<br>If its limit sample is needed, it can be fixed mutually with a customer.</td><td>Major</td></tr>
</table>

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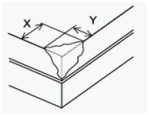
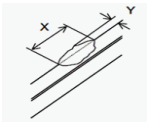
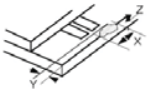
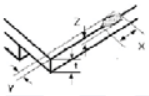
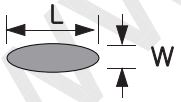
<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td rowspan="3">9</td><td>Glass Chipping<br>  <br> <br>[Pad area]</td><td>These criteria are applied to all corners of panel glass (unit : mm)<br><table><tr><td></td><td>Z</td><td>X</td><td>Y</td></tr><tr><td>Non-pad area</td><td>≦ t</td><td>≦ 1.0</td><td>≦ 1.0</td></tr><tr><td>Pad area</td><td>≦ t</td><td>≦ 2.0</td><td>≦ 1.2</td></tr></table>* Pad means the contact edge, overhung single glass part</td><td>Major</td></tr>
<tr><td>  </td><td>These criteria are applied to all side edges of panel glass (unit : mm)<br><table><tr><td>Z</td><td>X</td><td>Y</td></tr><tr><td>≦ t</td><td>≦ 2.0</td><td>≦ 0.5</td></tr></table></td><td>Major</td></tr>
<tr><td>  <br>[Front]<br>  <br>[Opposite]</td><td>These criteria are applied to only sides of pad area of panel glass (unit : mm)<br><table><tr><td colspan="2"></td><td>Z</td><td>X</td><td>Y</td></tr><tr><td rowspan="2">Pad front side</td><td>Near Pattern</td><td>≦ t</td><td>≦ 5.0</td><td>≦ 0.4</td></tr><tr><td>No Pattern</td><td>≦ t</td><td>≦ 5.0</td><td>≦ 0.5</td></tr><tr><td colspan="2">Pad opposite side</td><td>≦ t</td><td>≦ 5.0</td><td>≦ 0.6</td></tr></table></td><td>Major</td></tr>
</table>

### 13-3-2. Window

<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>1</td><td>Window Black/White Spots (Circular Foreign Material)<br>  <br>Ø=(L+W)/2</td><td><table><tr><td rowspan="2">Size Ø (mm)</td><td colspan="2">Acceptable number</td></tr><tr><td>V/A</td><td>Out of V/A (BM area)</td></tr><tr><td>Ø ≦ 0.15</td><td>Ignore</td><td>Ignore</td></tr><tr><td>0.15 < Ø ≦ 0.25</td><td>2</td><td>2</td></tr><tr><td>0.25 < Ø</td><td>0</td><td>0</td></tr></table>Note : In case a foreign material is removed with a soft cloth, it is ignored.</td><td>Major</td></tr>
<tr><td>2</td><td>Window Dent / Bubble</td><td><table><tr><td rowspan="2">Size Ø (mm)</td><td colspan="2">Acceptable number</td></tr><tr><td>V/A</td><td>Out of V/A (BM area)</td></tr><tr><td>Ø ≦ 0.15</td><td>Ignore</td><td>Ignore</td></tr><tr><td>0.15 < Ø ≦ 0.25</td><td>2</td><td>2</td></tr><tr><td>0.25 < Ø</td><td>0</td><td>0</td></tr></table></td><td>Major</td></tr>
</table>

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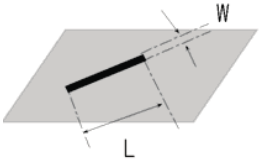
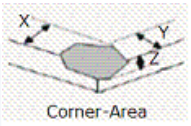
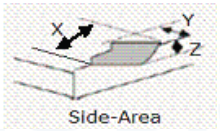
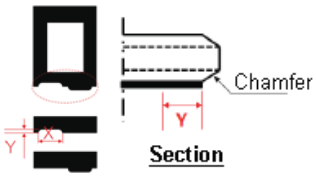
<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>3</td><td>Window Scratch<br> 
</td><td>
<table>
<tr><th>Width (㎜)</th><th>Length (㎜)</th><th>Acceptable number</th></tr>
<tr><td>W ≦ 0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td rowspan="2">0.03 < W ≦ 0.05</td><td>L ≦ 2.0</td><td>Ignore</td></tr>
<tr><td>2.0 < L ≦ 5.0</td><td>1</td></tr>
<tr><td rowspan="2">0.05 < W ≦ 0.08</td><td>L ≦ 1.0</td><td>Ignore</td></tr>
<tr><td>1.0 < L ≦ 4.0</td><td>1</td></tr>
<tr><td>0.08< W</td><td>Apply to Dent/Bubble</td><td>-</td></tr>
</table>
</td><td>Major</td></tr>
<tr><td>4</td><td>Window<br>(Line-shaped Foreign Material)</td><td>
<table>
<tr><th>Width (㎜)</th><th>Length (㎜)</th><th>Acceptable number</th></tr>
<tr><td>W ≦ 0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td rowspan="2">0.03 < W ≦ 0.05</td><td>L ≦ 2.0</td><td>Ignore</td></tr>
<tr><td>2.0 < L ≦ 5.0</td><td>1</td></tr>
<tr><td rowspan="2">0.05 < W ≦ 0.08</td><td>L ≦ 1.0</td><td>Ignore</td></tr>
<tr><td>1.0 < L ≦ 4.0</td><td>1</td></tr>
<tr><td>0.08< W</td><td>Apply to Spots (Circular Foreign Material)</td><td>-</td></tr>
</table>
</td><td>Major</td></tr>
<tr><td>5</td><td>Window Chipping</td><td>




<table>
<tr><th></th><th>X</th><th>Y</th><th>Z</th><th>Acceptable number</th></tr>
<tr><td>Front</td><td>X≦1.0</td><td>Y≦0.35</td><td></td><td rowspan="2">Total 2</td></tr>
<tr><td>Side/Corner/Back</td><td>X≦1.0</td><td>Y≦0.16</td><td>Z≦1/2t</td></tr>
</table>
</td><td>Major</td></tr>
<tr><td>6</td><td>Window Printing Defect</td><td>
<table>
<tr><th>Location</th><th>Size</th><th>Acceptable Number</th></tr>
<tr><td rowspan="3">Printing Inside</td><td>D ≦ 0.1</td><td>Ignore</td></tr>
<tr><td>0.1 < D ≦ 0.2</td><td>2</td></tr>
<tr><td>D > 0.2</td><td>0</td></tr>
<tr><td rowspan="3">Printing Outside</td><td>Y ≦ 0.1</td><td>Ignore</td></tr>
<tr><td>X≦1.5, 0.1<Y≦0.15</td><td>1</td></tr>
<tr><td>X>1.5, or Y>0.15</td><td>0</td></tr>
</table>
[Inside]<br>

D=(X+Y)/2<br>[Outside]<br> 

Note : These criteria are applied to each side<br>Note : Pinhole of the BM area follow the inside criteria</td><td>Major</td></tr>
</table>

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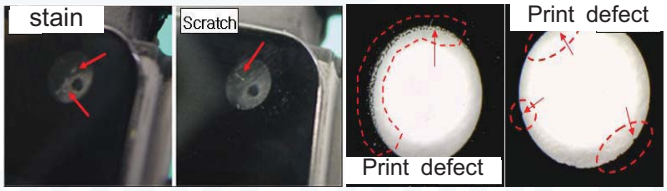
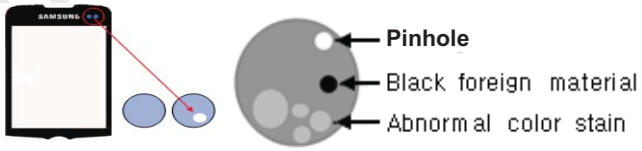
<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>7</td><td>Window Logo Area Printing Defect</td><td>N.A</td><td>Major</td></tr>
<tr><td>8</td><td>Window Icon Foreign Material</td><td>N.A</td><td>Major</td></tr>
<tr><td>9</td><td>Window Camera Hole</td><td>Foreign material/Stain/Scratch/Printing defects<br>1) Not allowed at Camera Hole center area<br>2) Allowed at Edge Area Printing Face : within 0.15mm<br> 
</td><td>Major</td></tr>
<tr><td>10</td><td>Window IR Sensor Area</td><td>
<table>
<tr><th></th><th>Defect Mode</th><th>Size (mm)</th><th>Acceptable Number</th></tr>
<tr><td>1</td><td>Pinhole</td><td>Φ≦0.15</td><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">Black Foreign Material</td><td>Φ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1<Φ≦0.15</td><td>1</td></tr>
<tr><td>3</td><td>Abnormal Color Stain</td><td>Φ≦0.3</td><td>Ignore</td></tr>
</table>


</td><td>Major</td></tr>
<tr><td>11</td><td>Surface Contamination</td><td>There should be no surface contamination which cannot be removed when being cleaned with a soft cloth.</td><td>Major</td></tr>
<tr><td>12</td><td>Icon Color Variation (Transparency)</td><td>N.A</td><td>Major</td></tr>
<tr><td>13</td><td>IR Color Variation (Transparency)</td><td>If Transparency is satisfied : allowed<br>Inspection mode : Transmittance(Light intensity : 400lux)</td><td>Major</td></tr>
</table>



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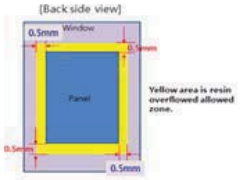
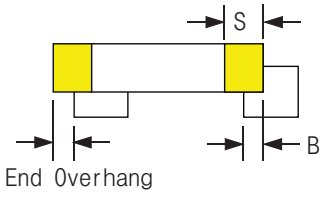
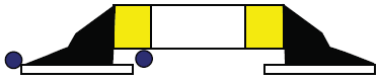
### 13-3-3. Other

| No. | Item | Criterion of Defect | Type |
|---|---|---|---|
| 1 | Lamination | Resin cleaning marks (no height difference): Allowed<br>Resin overflow /residues: 0.5mm allowed from each edge of a panel  <br>Resin bubble: Not allowed. (If its limit sample is needed, it can be fixed mutually.) <br>Resin non-application (under viewing/active area): Not allowed<br>Resin Vertical Pit: Not allowed | Major |
| 2 | FPCA SMT(Soldering) | (1) No polarity opposition<br>(2) No wrong insertion | Major |
| 3 | FPCA Solder Short | Short of proximity pattern and land is defect | Major |
| 4 | FPCA Solder Crack | There should be no crack which gives an effect to quality of the display | Major |
| 5 | FPCA End Overhang | The size above 1/2 of soldering electrode of the parts overhang to the LAND is prohibited<br>(but, contacting near other components is prohibited.)   | Major |
| 6 | FPCA Solder Ball | Not allowed if (Φ> 150um)  | Major |

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<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>7</td><td>FPCB<br>(Dent/Scratch)</td><td>(1) Open Area : Not allowed if Cu layer exposed.<br>(2) Solder mask Area : Not allowed if Cu layer exposed.<br>(3) Pattern Area : Not allowed if Cu layer exposed.<br>(4) Black shield Area:
<table>
<tr><th>Defect Mode</th><th>Size</th><th>Acceptable Number</th></tr>
<tr><td>Line shaped</td><td>L ≦ 5mm</td><td>Ignore</td></tr>
<tr><td rowspan="2">Spot / Face Shaped</td><td>S(Area) ≦0.6mm$^2$</td><td>Ignore</td></tr>
<tr><td>0.6mm$^2$ < S(Area) < 1.0mm$^2$</td><td>2 Point</td></tr>
</table></td><td>Major</td></tr>
<tr><td>8</td><td>FPC Tilt Defect</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>9</td><td>TSP Function NG</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>10</td><td>Black Tape Bubble</td><td>If it's not seen at the front side : allowed.</td><td>Major</td></tr>
<tr><td>11</td><td>Black Tape Dent</td><td>If it's not seen at the front side : allowed.</td><td>Major</td></tr>
<tr><td>12</td><td>window cover film<br>(protect film)</td><td>Cover film shall not be located out of the window area.<br>Cover film shall not be torn, made a hole.</td><td>Major</td></tr>
</table>

※ Other cosmetic items which are not defined above are allowed, if they are not seen at the front side after assembling phone set.

But, they follow the SDC's criteria, if SDC has one.

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# 14. Reliability

## 14-1. Environmental test

| No | Item | Condition | qnty | Result | Judgment Criterion |
|---|---|---|---|---|---|
| 1 | Temperature Humidity Bias | 60℃/93%RH/ 120 hrs | 10 | | 1. No clearly visible defects or remarkable deterioration of display quality.However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted.<br>2. No function-related abnormalities<br>3. Optical criteria :<br>.White △u'v' ≤0.02 |
| 2 | Wet High Temperature Storage | 60℃/93%RH/ 120 hrs | 10 | | |
| 3 | High Temperature Storage | 85℃/ 120 hrs | 5 | | |
| 4 | Low Temperature Stroage | -40℃ 120 hrs | 5 | | |
| 5 | Thermal Shock | 85℃1hr - -40℃ 1hr / 30 cycle | 10 | | |

Note) The results must be measured after 2 hours later under room temperature keeping.

## 14-2. Electrical test

| No. | Item | Condition | qnty | Result | Judgment Criterion |
|---|---|---|---|---|---|
| 1 | ESD | -Air discharge : ±8kV, 5POINT, Each 2times<br>-Contact discharge : ±4kV, 5POINT, Each 2times | 5 | | 1. No visible defects .(optical / mechanical)<br>2. No function-related abnormalities |

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# 15. Handling Precautions

## 15-1. Mounting Method

The AMOLED panel of SAMSUNG Display CO.,LTD. module consists of two slim glasses with polarizer which can easily get damaged. Since the module is constructed as to be fixed by utilizing fitting holes in the printed circuit board. Extreme care should be used when handling the AMOLED modules.

## 15-2. Caution of AMOLED Handling and Cleaning

When cleaning the display surface, use soft cloth solvent as recommended below and wipe gently.

◎ Isopropyl alcohol
◎ Ethyl alcohol
◎ Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent.

◎ Water
◎ Ketone
◎ Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns.
Do not use the following solvent on the pad and prevent it from being contaminated.

◎ HCFC (Other area except ITO pad can use the HCFC for cleaning process)
◎ Soldering flux
◎ Chlorine(Cl), Sulfur(S)
◎ Spittle, Fingerprint

If the product is not wrapped with a desiccant added pad, ITO pattern can be damaged by corrosion. SAMSUNG Display CO,.LDT. suggests wrapping a product with a desiccant unless customers particularly indicate that they do not want it. In case ITO pattern corrodes due to the usage of chlorine, sulfur or customer's mishandling of the product, the responsibility lies with the customer.

## 15-3. Caution Against Static Charge

For AMOLED module, use C-MOS LSI drivers, therefore we recommend that you ;
Connect any unused input terminal to VCI or VSS, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects AMOLED.
Against static charge, you should make sure that the product is safe or not by experiment in advance.

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## 15-4. Packing

◎ The packing principle is that AMOLED module should keep its packing condition at the time of delivery.

◎ For safety & avoiding the module damage, Carton box must stack the below 4 boxes. When storing the AMOLED after unpacking, note the followings.

◎ AMOLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.

◎ To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

## 13-5. Caution for Operation

◎ If you do not follow normal POWER ON , OFF sequence or abnormal operating, then AMOLED module can be damaged electro-optically and does not recover.
Do not change software without Samsung Display confirmation.

◎ Response time may extremely delay at a temperature lower than operating range, AMOLED does not normally operate at a high temperature. But this may recover at a proper temperature.

◎ When you set optimal operating voltage to AMOLED module, you can see the optimal contrast of AMOLED. So, add voltage controllable function at SET Module.

◎ AMOLED module may not display normally when twisting power or pressing power is added. Therefore you should secure AMOLED module maximum thickness at set assembly not to have any pressure affect AMOLED module.

◎ Electro-chemical reaction may occur when there is humidity on pad, therefore, you should use AMOLED Module below maximum operating humidity.

◎ AMOLED Module Power Vdd should be designed to protect surge current at SET Module.

◎ You should not damage connector and cable for AMOLED module assembly by force folding or by applying extreme power.

◎ AMOLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage AMOLED module by surrounding elements.

◎ To satisfy EMI standards, you should plan your design after considering emitting energy.

◎ We can not guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area.

◎ Image-sticking may occur if AMOLED displays same image for a long time, so you need to make a change for AMOLED.

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## 15-6. Storage

◎ Place in a dark place where neither exposure to direct sunlight or any fluorescent light is permitted and keep at room temperature & room humidity.

◎ Store with no contact with polarizer surface.
[ It is recommended to store them as they have been contained in the inner container when we delivered them.]

## 15-7. Safety Precautions

◎ Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMOLED module, dust adhesion, or scratches on the display part.

◎ In the event that the contents of AMOLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary.

◎ Do not use the AMOLED module for the special purpose besides display units.

◎ Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken.

## 15-8. Precautions before Use

You should discuss the following case with SAMSUNG Display CO., LTD.

◎ in case of any questions about contents of this "Specification For Approval".

◎ in case of occurring new problems not mentioned at this "Specification For Approval".

◎ in case of your request about income inspection specification change.

◎ in case of occurring new problem at your driving test.

※ **If SAMSUNG Display CO., LTD has to change the conditions specified in the specification, previously the negotiation shall be held and decided.**

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# 16. Drawing

## 16-1. Product Drawing

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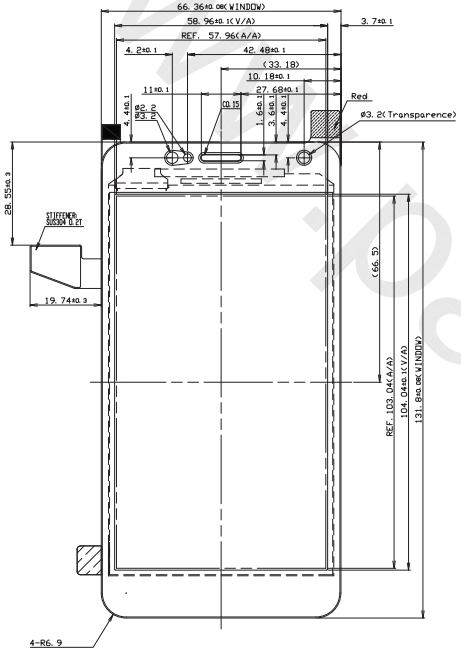
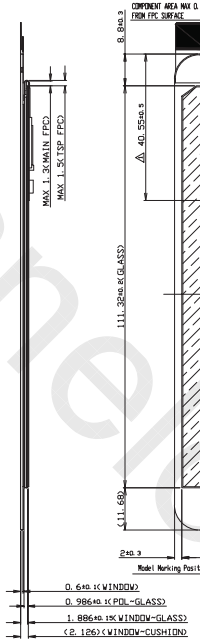
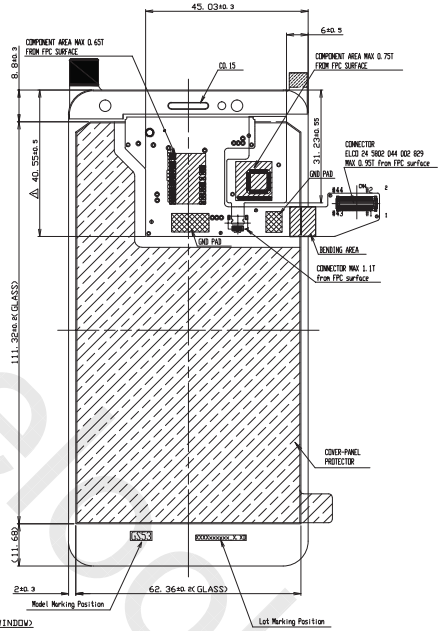
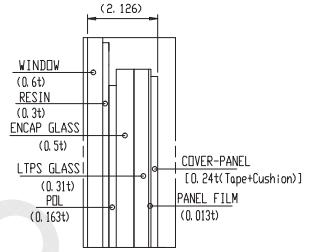



| Pin number | Pin name |
|---|---|
| 1 | GND |
| 2 | GND |
| 3 | D3_N |
| 4 | RESX |
| 5 | D3_P |
| 6 | NC |
| 7 | GND |
| 8 | VDD3.2.2V |
| 9 | D0_N |
| 10 | VCI_3.3V |
| 11 | D0_P |
| 12 | TSP_VDD_3.3V |
| 13 | GND |
| 14 | MTPHV |
| 15 | CLK_N |
| 16 | EL_ON |
| 17 | CLK_P |
| 18 | NC |
| 19 | GND |
| 20 | GND |
| 21 | D1_N |
| 22 | TSP_SCL |
| 23 | D1_P |
| 24 | TSP_SDA |
| 25 | GND |
| 26 | GND |
| 27 | D2_N |
| 28 | TSP_INT |
| 29 | D2_P |
| 30 | GND |
| 31 | GND |
| 32 | GND |
| 33 | NC |
| 34 | NC |
| 35 | ELVDD |
| 36 | ELVSS |
| 37 | ELVDD |
| 38 | ELVSS |
| 39 | ELVDD |
| 40 | ELVSS |
| 41 | GND |
| 42 | GND |
| 43 | GND |
| 44 | GND |

[PIN MAP]




[STACK UP(Scale: N/S)]

NOTE

1. DESCRIPTION : 4.65"HD720 (1280X720)AMOLED DISPLAY
2. THIS MODULE IS ACCORDING TO ENVIRONMENTAL REQUIREMENTS(ROHS).

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3) ALL RIGHTS RESERVED

| REV | DATE | DESCRIPTION OF REVISION | REASON |
|---|---|---|---|
| '001 | '13. 07. 11 | ⚠Modify 'Window Edge-Main-FPC Edge' Tolerance | |

CHK'D BY

| GENERAL TOLERANCE | | | |
|---|---|---|---|
| STEP | LEV. 1 | LEV. 2 | LEV. 3 |
| 0 < X ≤ 6 | ±0.05 | - | - |
| 6 < X ≤ 30 | ±0.10 | - | - |
| 30 < X ≤ 60 | ±0.12 | - | - |
| 60 < X ≤ 120 | ±0.15 | - | - |
| 120 < X ≤ 180 | ±0.20 | - | - |
| 180 < X ≤ 300 | ±0.25 | - | - |

| UNIT | mm |
|---|---|
| SCALE | 1:1 |
| TOLERANCE | |
| LEV. 1 | |

| DES'D BY | CHK'D BY | APP'D BY |
|---|---|---|
| J. C. PARK | D. H. CHO | J. S. OH |
| '13. 07. 11 | '13. 07. 11 | '13. 07. 11 |

SAMSUNG DISPLAY

| PROJECTION | STD. TOL | SIZE |
|---|---|---|
| | - | A2 |

| | | | |
|---|---|---|---|
| MODEL NAME | AMS465GS53 | | |
| PART NAME | OUTLINE DIMENSION | | |
| CODE NO. | - | SHEET | 1/1 |
| SPEC NO. | - | VER | 001 |

2013. 07. 11 / Mechanical Component Development Group(OLED) / PARK JAE CHUN

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## 16-2. Main FPCB Drawing

### 16-2-1. Main FPC Schematic Diagram

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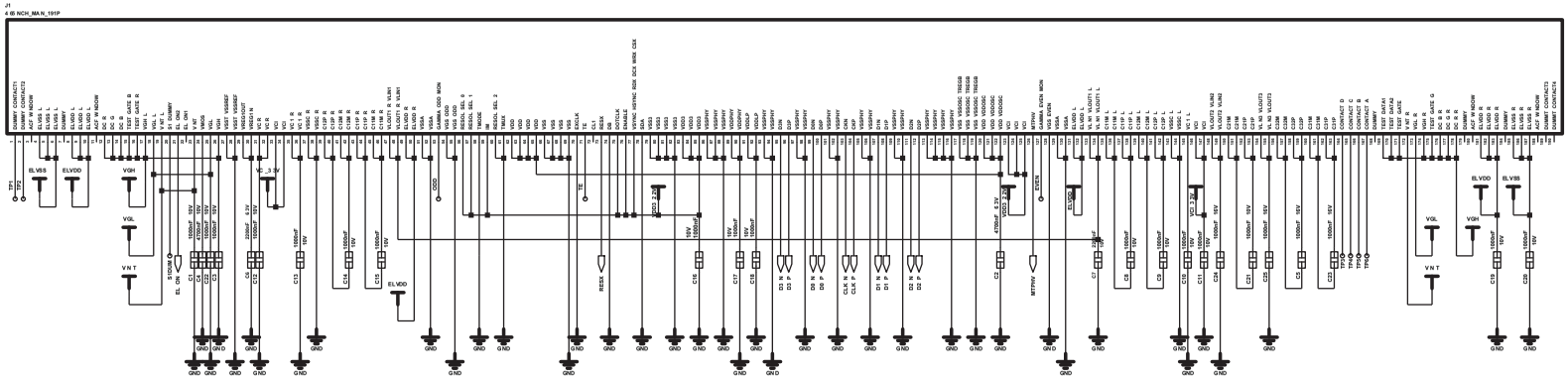

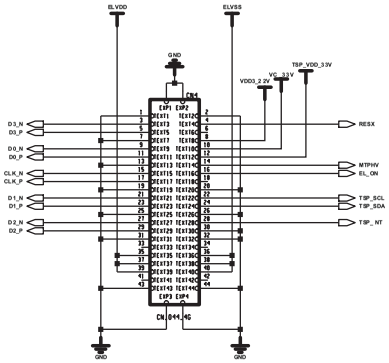


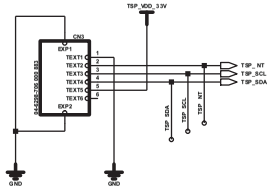


| RESOL_SEL<2> | RESOL_SEL<1> | RESOL_SEL<0> | Resolution |
|---|---|---|---|
| 0 | 0 | 0 | 540 x 960 |
| 1 | 0 | 1 | 800 x 1280 |

| LANE_SEL<1> | LANE_SEL<0> | MIPI Lane Select |
|---|---|---|
| 0 | 1 | 2 LANE |
| 1 | 1 | 4 LANE |

| | | |
|---|---|---|
| Changed by: C.S.SON | Date: 2011/10/24 | Time: 9:12:46 |
| Engineer: J.H.KIM | Drawn By: C.S.SON | R&D CHK |

| | |
|---|---|
| Spec No. | ODS01584-000 |
| Part Name | ASSY FPC-MAIN |
| PBA Code | LJ94-26160A |
| Sheet | 1/1 [A3] |

**Samsung Mobile Display**

SPECIFICATION — **AMS465GS16 MAIN REV1.2**

## 16-2-2. Main FPC Electronic Part List

| NO | CATEGORY | REFERENCE | Q'ty | SPECIFICATION | SMD CODE | MAKER |
|---|---|---|---|---|---|---|
| 1 | C-CER,CHIP | C1,C3,C8~C22 | 17 | 1000nF,10%,10V,X5R,TP,1005 | 2203-006562 | Note 1 |
| 2 | C-CER,CHIP | C5,C23~25 | 4 | 1000nF,10%,16V,X5R,TP,1005 | 2203-006841 | Note 1 |
| 3 | C-CER,CHIP | C6 | 1 | 2200nF,10%,6.3V,X5R,1005 | 2203-006838 | Note 1 |
| 4 | C-CER,CHIP | C7 | 1 | 2200nF,10%,10V,X5R,TP,1005 | 2203-007271 | Note 1 |
| 5 | C-CER,CHIP | C2 | 1 | 4700nF,20%,6.3V,X5R,TP,1005 | 2203-007317 | Note 1 |
| 6 | C-CER,CHIP | C4 | 1 | 4700nF,10%,10V,X5R,TP,1005 | 2203-007393 | Note 1 |
| 7 | SOCKET-BOARD TO BOARD | CN4 | 1 | 24-5802-044-002-829,44P,2R,0.4MM,SMD-S,AU,BL | 3710-002685 | ELCO |
| 8 | CONNECTOR-FPC/FFC/PIC | CN3 | 1 | 04-6298-706-000-883,6P,0.5mm,SMD-A,Au,ZIF,FLIP,BOTTOM | 3708-002015 | ELCO |
| 9 | FPC | FPCB | 1 | AMS465GS16 Main Rev1.2 | LJ41-10486A | BH-Flex |
| 10 | Main TAPE #1 | - | 1 | Adhesive : SEKISUI 3805H (0.05t)<br>Remover : KERN 91754B (0.075 blue) | - | |

1) NOTE 1 : AVX/KYOCERA, MURATA, TAIYO YUDEN, TDK, SEM

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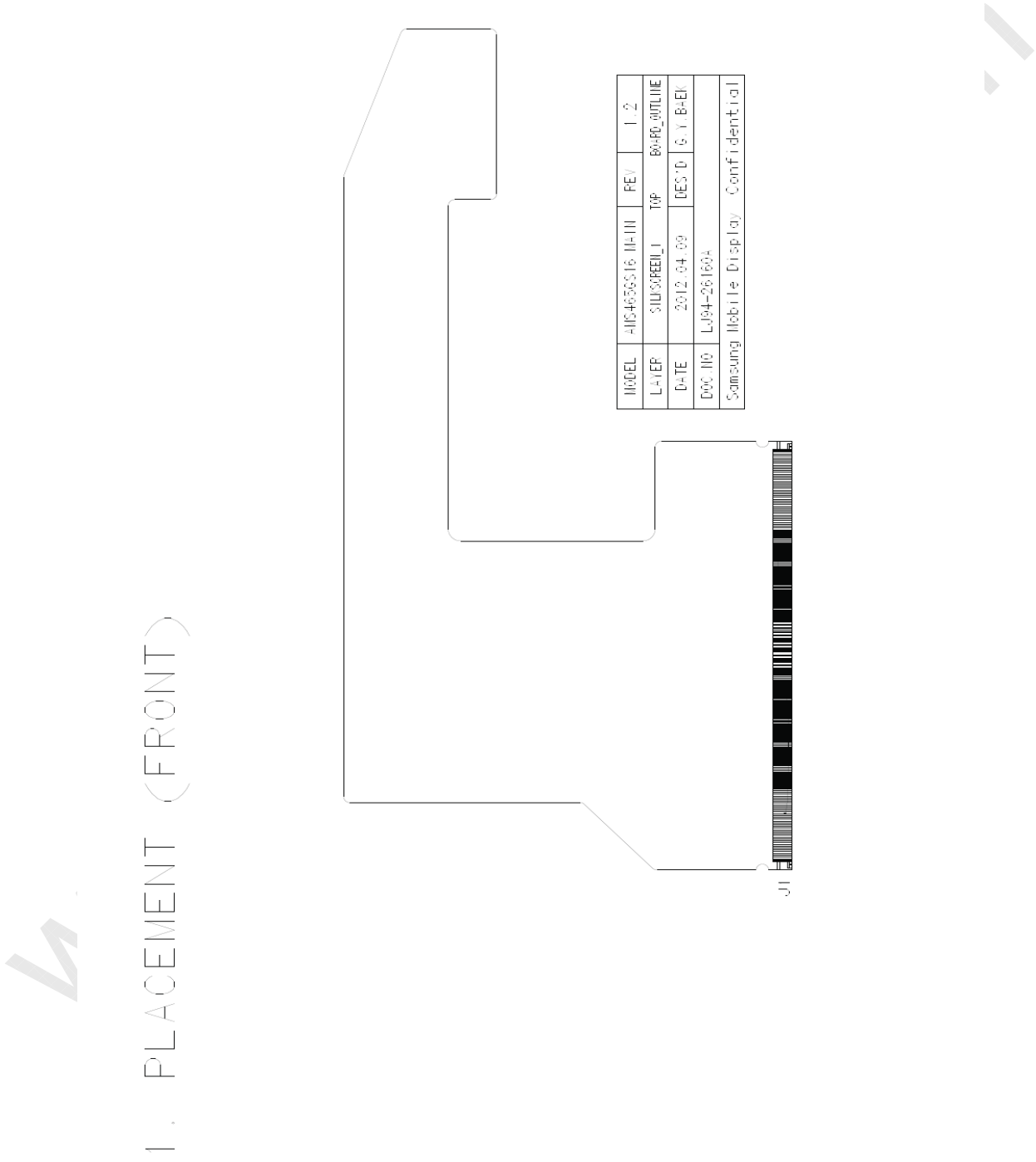
## 16-2-3. Main FPC Placement (Front)



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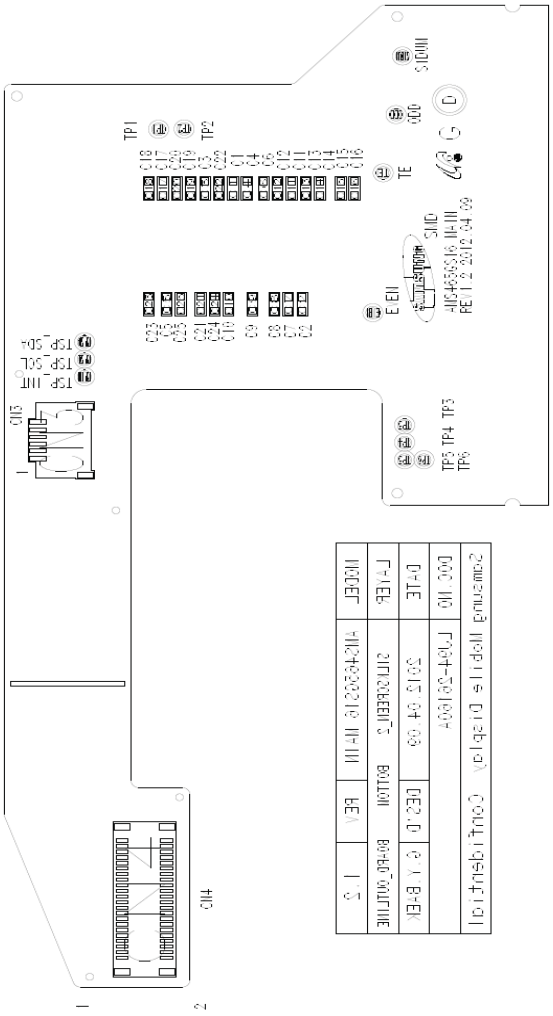
## 16-2-4. Main FPC Placement (Rear)



1. PLACEMENT (REAR)

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## 16-3. TSP FPCB Drawing

### 16-3-1. TFPC Schematic Diagram

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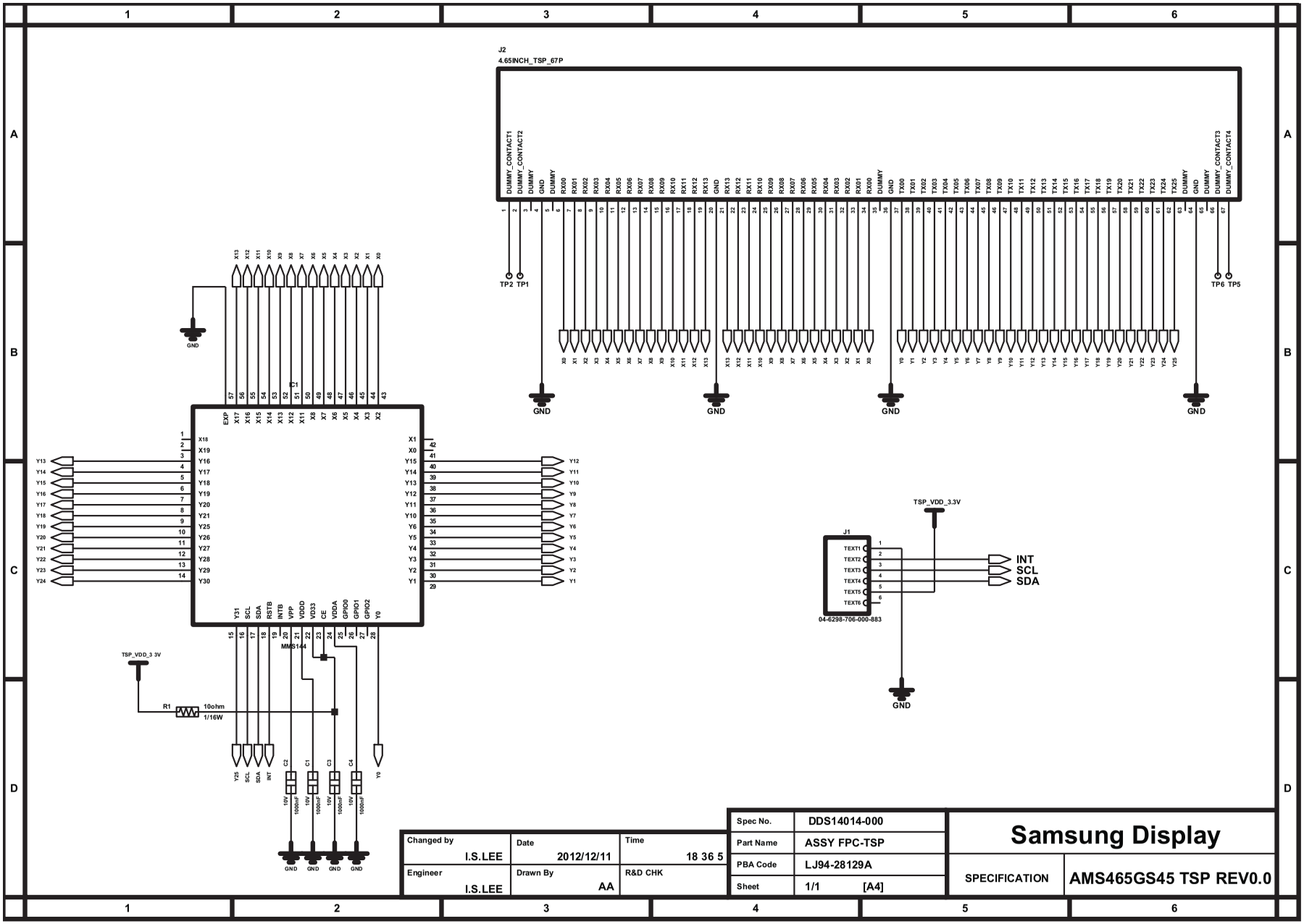


| | | | |
|---|---|---|---|
| Changed by | I.S.LEE | Date | 2012/12/11 |
| Time | 18 36 5 | | |
| Engineer | I.S.LEE | Drawn By | AA |
| R&D CHK | | | |

| | |
|---|---|
| Spec No. | DDS14014-000 |
| Part Name | ASSY FPC-TSP |
| PBA Code | LJ94-28129A |
| Sheet | 1/1 [A4] |

**Samsung Display**

SPECIFICATION — AMS465GS45 TSP REV0.0

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## 16-3-2. TSP FPC Electronic Part List

| NO | CATEGORY | REFERENCE | SPECIFICATION | SMD CODE | MAKER |
|---|---|---|---|---|---|
| 1 | IC-MICROCONTROLLER | IC1 | MMS144,QFN,56P,6*6*0.5,TP,2.8V,-40to+85C Ver5.4 | 0903-001887 | MELFAS |
| 2 | C-CER,CHIP | C1~C4 | 1000nF,10%,10V,X5R,TP,1005 | 2203-006562 | Note 1 |
| 3 | R-CHIP | R1 | 10ohm,1%,1/16W,TP,1005 | 2007-007798 | |
| 4 | FPC | FPCB- | ASM465GS45 Touch Fpcb Rev0.0 | LJ41-11165A | BH-Flex |

1) NOTE#1 : AVX/KYOCERA, MURATA, TAIYO YUDEN, TDK, SEM
2) All Components H/F.

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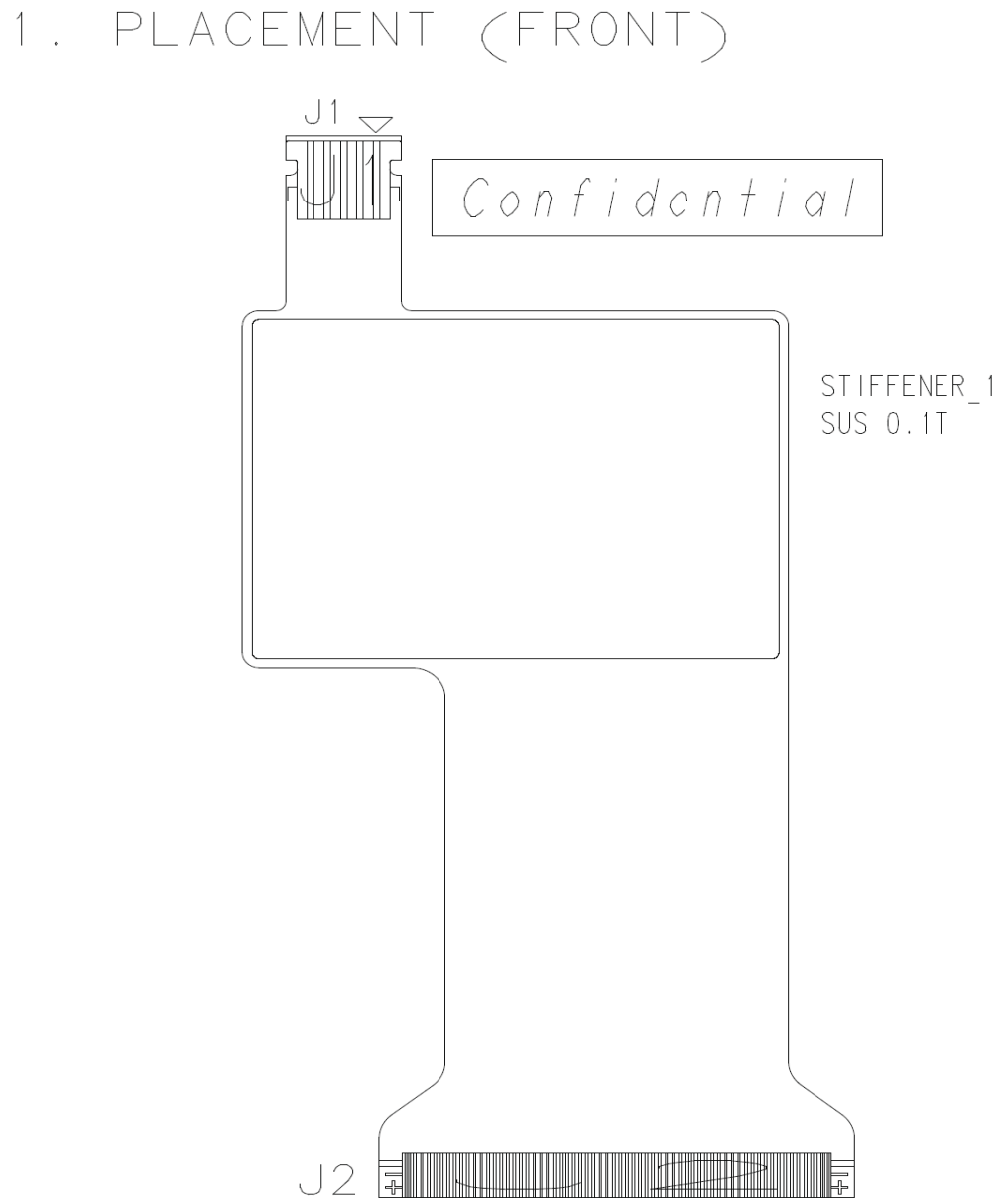
### 16-3-3. TSP FPC Placement (Front)




| | | | |
|---|---|---|---|
| MODEL | AMS465GS45 TSP | REV | 0.0 |
| LAYER | STIFFENER_1 TOP | | BOARD_OUTLINE |
| DATE | 2012.12.11 | DES'D | C.S.SON |
| DOC.NO | LJ94-28129A | | |
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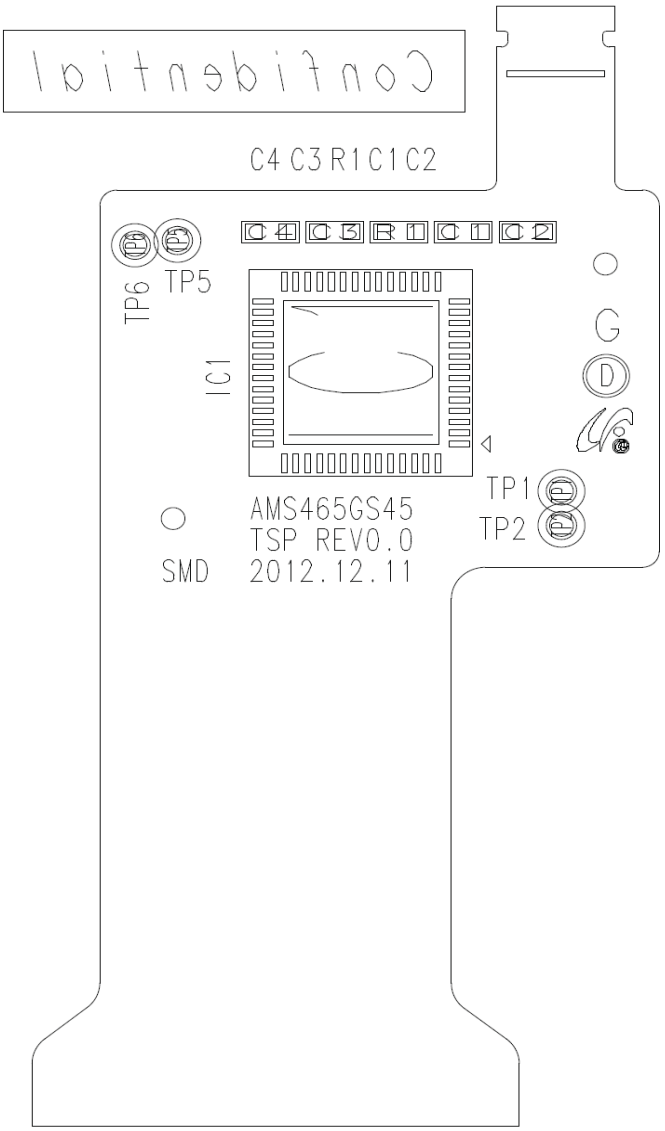
### 16-3-4. TSP FPC Placement (Rear)

1. PLACEMENT (REAR)




| | | | |
|---|---|---|---|
| MODEL | AMS465GS45 TSP | REV | 0.0 |
| LAYER | SILKSCREEN_2 BOTTOM | | BOARD_OUTLINE |
| DATE | 2012.12.11 | DES'D | C.S.SON |
| DOC.NO | LJ94-28129A | | |
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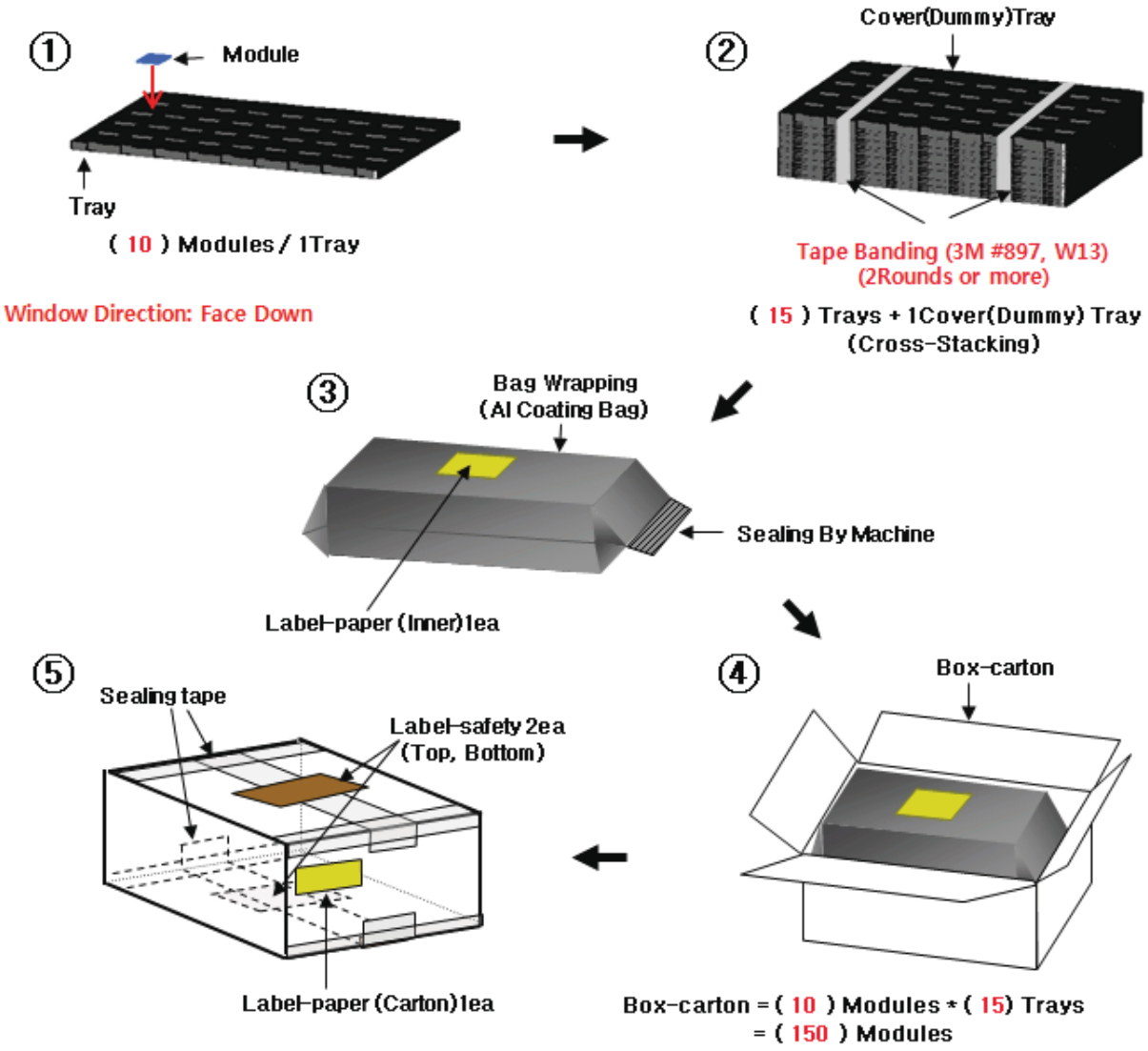
# 17. Packing Specification

## 17.1 Box Pack




**Note**

(1) Total :Box-carton approx. : ( 10.5 )kg

(2) Size : 583(L) x 388(W) x 210(H)

(3) Place the Module in the tray facing the active area direction.

(4) Stack the trays and cover (dummy) tray.

(5) Resistance of tray surface : $10^6$~$10^9\Omega$

(6) Wrap the Al coating bag by Packing machine and affix the Label-Paper on Bag

(7) Put the bag in the Box-carton .

(8) Seal the Box-carton and affix the Label-safety & Label-paper.

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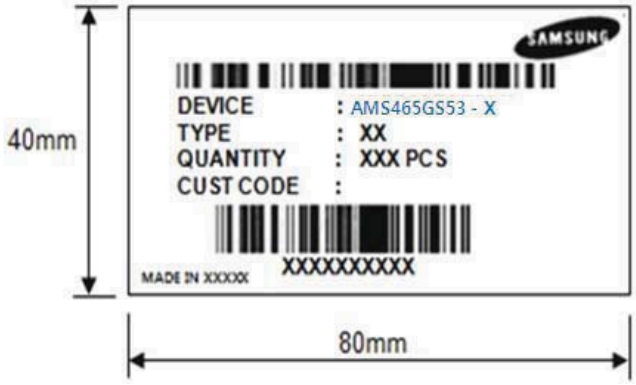
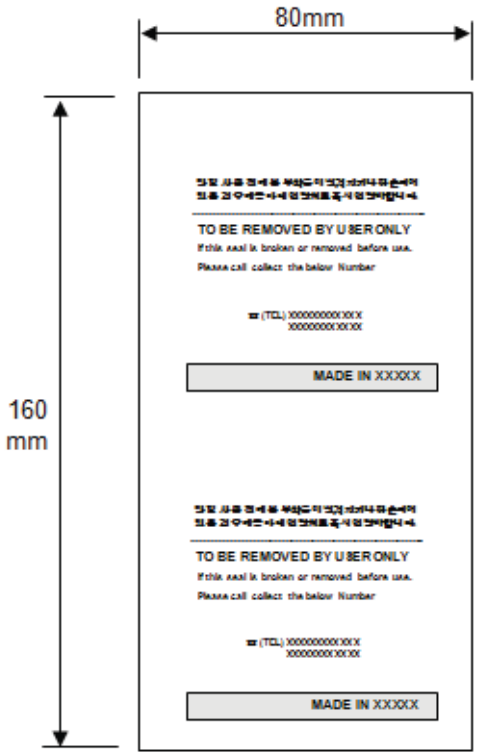
## 17.2 Label

* Label-paper (Inner)




* Label-paper (Carton)

* Label-safety

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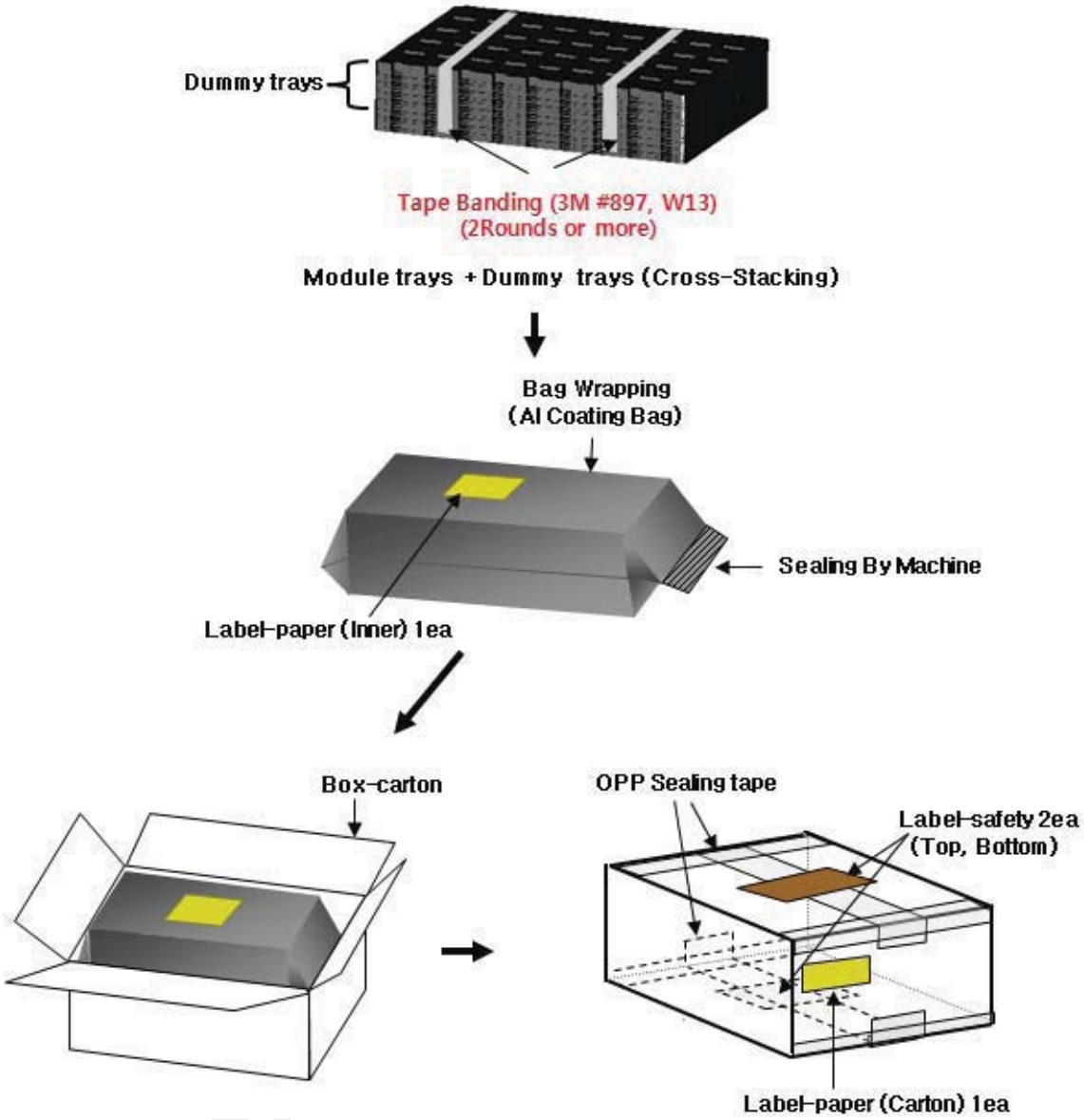
## 17.3 Packing for Small Quantities




**Note**

When package quantity is small, Modules containing trays are stacked the bottom, and dummy trays are stacked at the top of package,
then wrap the Al coating bag by Packing machine and affix the Label-Paper on Bag.
Put the Bag in the Box-carton
Seal the Box-carton and affix the Label-safety & Label-Paper.

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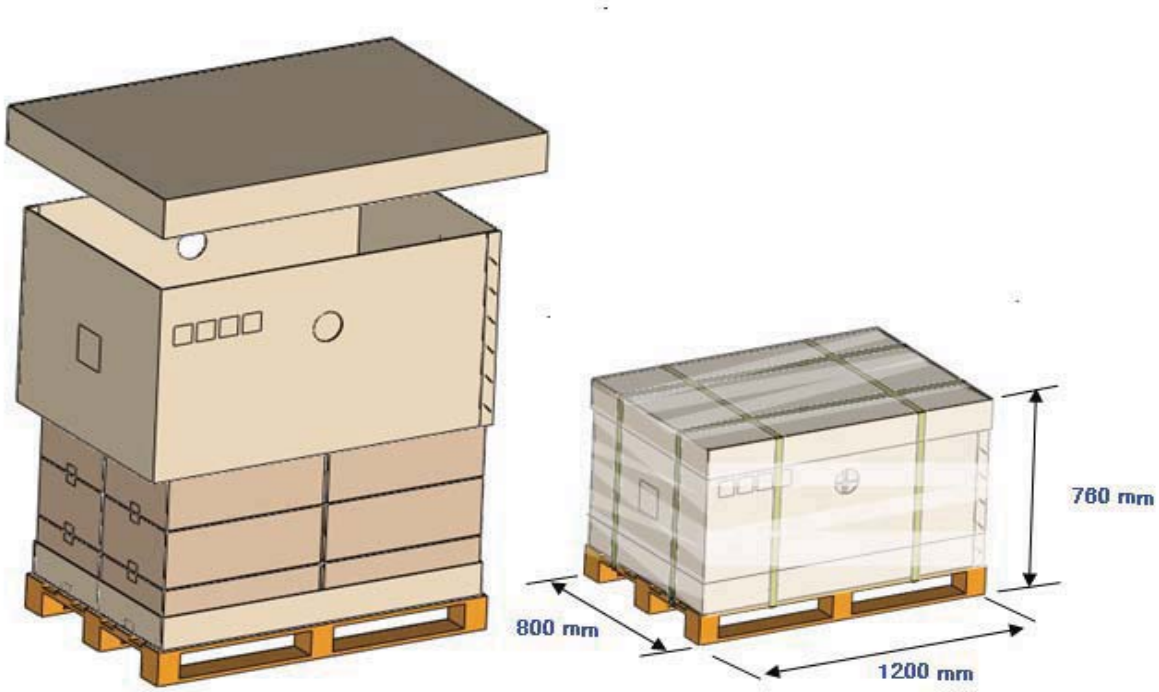
## 17.4 Over Pack

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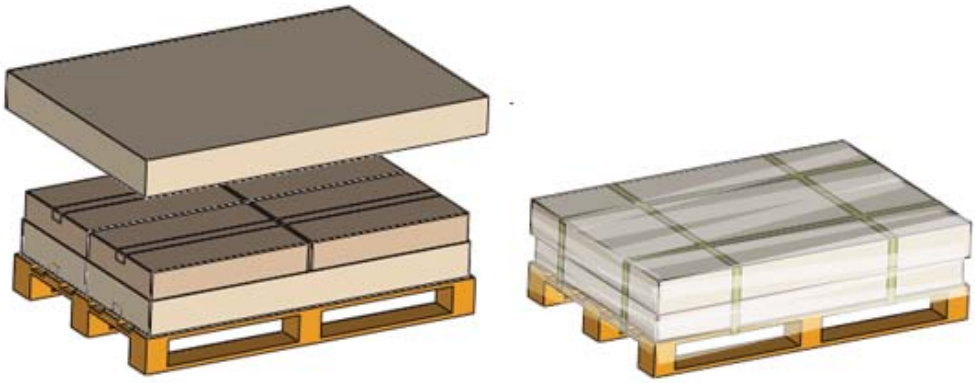
## 17.5 Packing for Small Quantities





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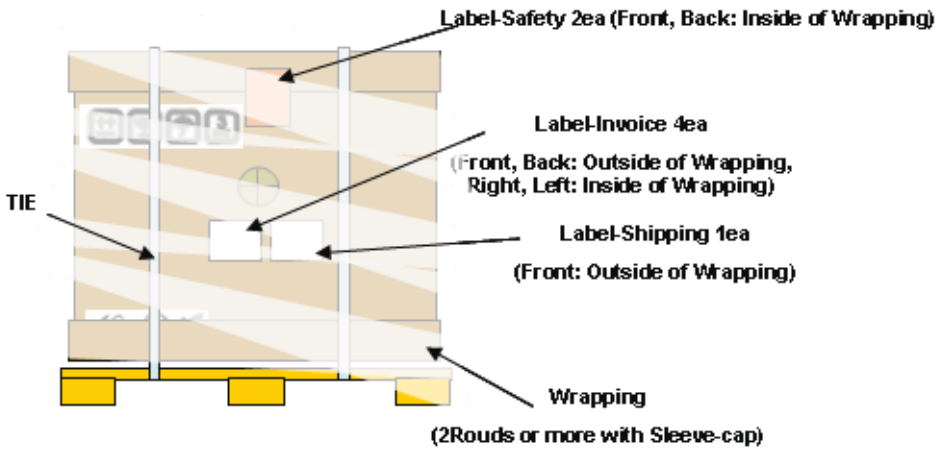
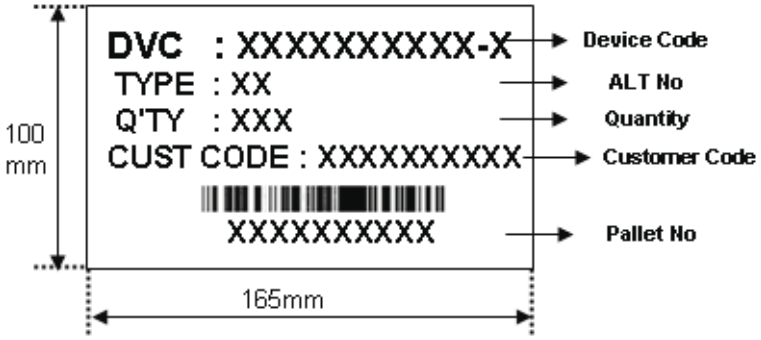
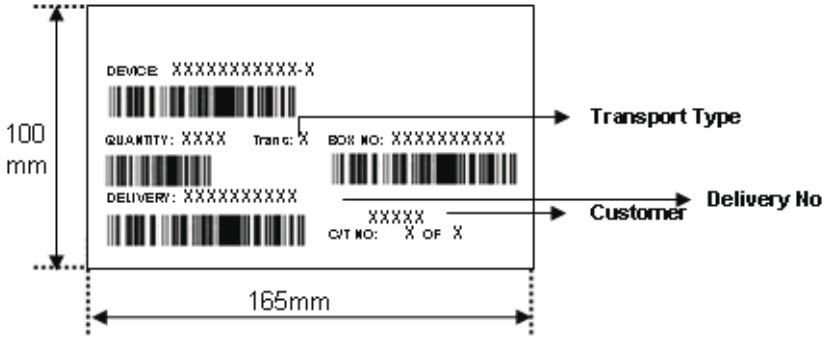
## 17.6 Over Pack Attach




* Label-invoice




* Label-shipping

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* Reference Image (Except Label and Wrap)

| | |
|---|---|
| Carton Box | |
| Sleeve Box | |

## Caution

For keeping safe quality from outer exposure or contamination, modules should be consumed in 2 months after unpacking.

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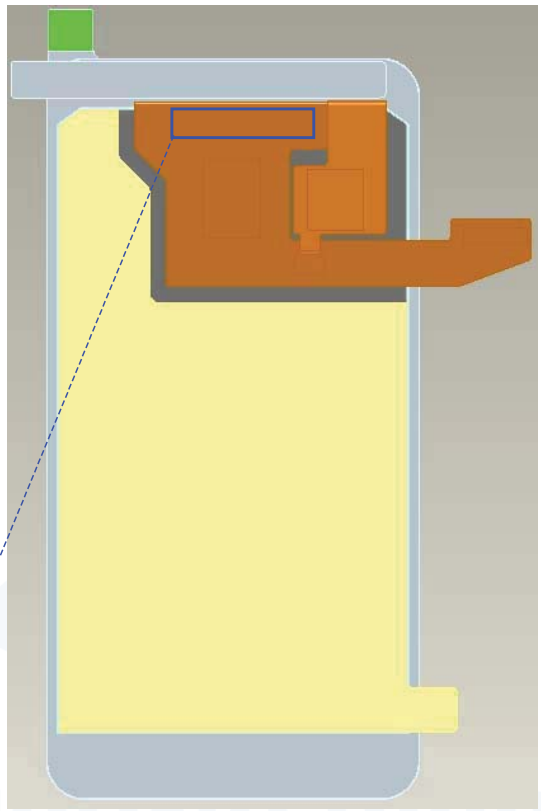
# 18.Module Marking



**$S_1...S_n$**
**$L_S$ $L_D$ YYMMDD $L_1L_2$ V**

| Digit code | Description | Example |
|---|---|---|
| $S_1...S_n$ | supplier's material code in n digits. | AMS465GS53-0 |
| $L_S$ | assembled site where sample was made.<br>A: Korea, D: Dongkwan in China, T: Tenjin in China | D |
| $L_D$ | assembled shift when sample was made.<br>A: A-shift(day), B: B-shift(night), C: C-shift | A |
| YYMMDD | the year, month and date when sample was made.<br>YY: year, MM: month, DD: date | 130527 |
| $L_1L_2$ | assembled line where sample was made.<br>01: 1-line, 02: 2-line, ... , 99: 99-line | 01 |
| V | sample version<br>W: W/S, E: E/S O: C/S or MP, P: PCN | O |

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